Research into the behaviour of SOI devices operating in extreme environments

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Year Report (Sept. 95-Sept. 96)

by:

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Contents

1. Irradiation of GAA analog circuits

The essential part of the work on the irradiation of GAA devices is presented in the Ph.D. thesis of Pascale Francis, entitled"*Double-gate SOI/MOS devices and circuits in hostile environments*", which can be found as an attachement to this report. This year, the irradiation response of analog (in contrast to digital) parameters and circuits were analyzed.

Analog parameters

In addition to the threshold voltage and the transconductance, the scaled transconductance g_m/I_D [V^{-1}] and the output conductance $g_D = I_D/V_{EA}$, with V_{EA} the equivalent Early voltage [1], are physical characteristics which are crucial for analog design. Indeed, considering a common-source MOS transistor operating in saturation and loaded by an ideal current source and an output capacitance C_L (Figure 1), it is well known that the transition frequency of the voltage amplification (the frequency where the open-loop gain is equal to unity) is given by $(g_m/I_D)(I_{bias}/2\pi C_L)$, while the D.C. voltage gain A_0 is equal to $(g_m/I_D)V_{EA}$. Variations of the noise characteristics with dose are important as well and can be found in Reference [2] for GAA devices.

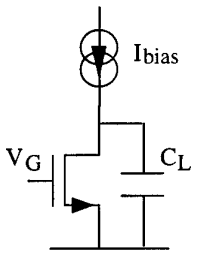

Figure 1: MOSFET in basic common-source amplifying configuration.

Scaled transconductance

The evolution of g_m/I_D as a function of the normalized drain current $I_D/(W/L)$ with dose as parameter is depicted in Figure 2 for devices irradiated with V_G = 3V. This parameter is independent on device dimensions and its value inversely follows the inversion level in the silicon film [3]. In weak inversion region, the maximum of the scaled transconductance is related to the subthreshold slope S by $(gm/I_D)_{max} = \ln(10)/S$. Since the pre-radiation value of S is close to the theoretical limit, $(gm/I_D)_{max}$

---

1 Y.P. Tsividis, "*Operation and modeling of the MOS transistor*", McGraw-Hill Book Company. New-York, 1987

2 E. Simoen, C. Claeys, S. Coenen, and M. Decreton, "D.C. and low frequency noise characteristics of γ-irradiated Gate-All-Around silicon-on-insulator MOS transistors", *Solid States Electronics*, vol. 38, no. 1, pp. 1-8, 1995

3 E.A. Vittoz, "Design of low-voltage low-power IC's", *Proc. ESSDERC*, pp. 927-934, Grenoble, 1993

before irradiation approaches q/kT = 38.4V^{-1}. Like the subthreshold slope, $(gm/I_D)_{max}$ degrades, as shown in Figure 3, and falls down to 30% and 50% of its initial value after 85Mrad(Si) irradiation in n- and p-channel devices respectively. The drop is more rapid in n-channel devices as expected from the larger interface state generation. The scaled transconductance in strong inversion operation (I_D > 1μA), on the contrary, is nearly not affected by dose up to 85Mrad(Si), and should follow the degradation of the square root of μ. The influence of the gate bias during irradiation is negligible in p-channel devices, and the degradation is slightly smaller with V_G = 0V in n-channel devices.

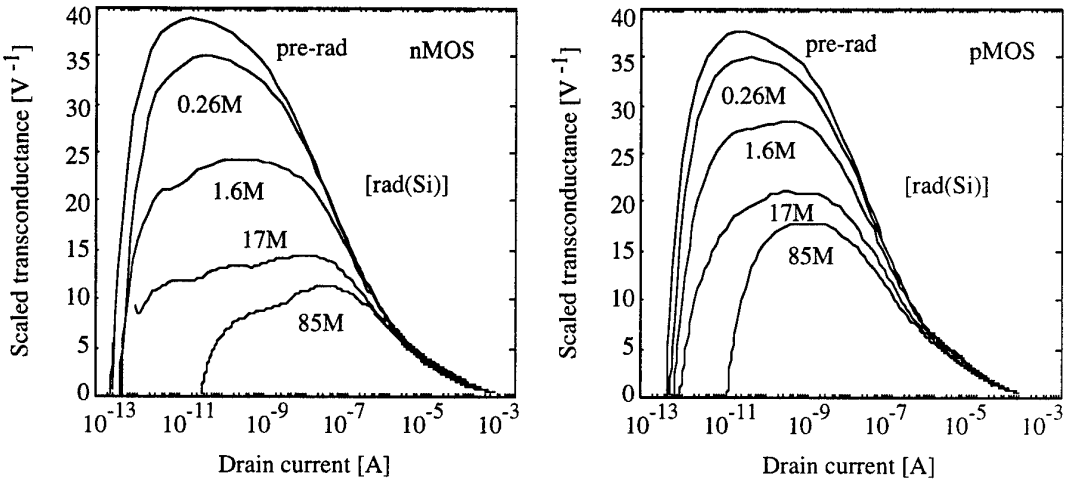

Figure 2: Scaled transconductance g_m/I_D as a function of the normalized drain current $I_D/(W/L)$ with dose as parameter in 3μm × 3μm n- and p- channel GAA devices irradiated with V_G = 3V.

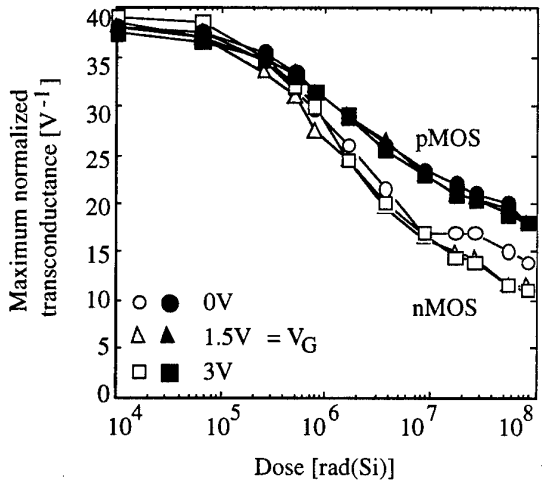

Figure 3: Maximum scaled transconductance of 3μm × 3μm n- and p- channel GAA devices as a function of dose with the gate bias applied during irradiation as parameter.

Output conductance

The output conductance g_D is obtained as the slope of the best linear regression on the flat portion of drain current *vs.* drain voltage curves. The lower boundary for V_D ensures that the device is in saturation regime while the upper boundary eliminates the region where impact ionization could appear. Since g_D depends on V_G, three different extraction methods, summarized in Table 5.3, are compared: in the first two cases, V_G is adapted to maintain a constant current level as a function of the dose; in the third case, V_G is kept constant.

Table 5.3: Summary of three different methods to extract the output conductance.

	Method 1	Method 2	Method3
nMOS	$I_D > 40\mu A$	$I_D > 80\mu A$	$V_G = 1.5V$
pMOS	$I_D > 10\mu A$	$I_D > 20\mu A$	$V_G = 1.75V$

The resulting Early voltages $V_{EA} = I_{D0}/g_D$ are shown in Figure 4 as a function of dose, with I_{D0} the drain current linearly extrapolated to V_G = 0V. Only small discrepancies appear between the three definitions of V_{EA}, the spread being more pronounced at low(high) doses in nMOS(pMOS) devices (Figure 3, left). The pre-rad value of V_{EA} is generally larger in n-channel (60...100V) than in p-channel devices (60...70V). V_{EAn} remains constant up to about 1Mrad(Si) and then severely drops towards a new stable value around 10...20V. The degradation is slightly worst but begins at higher dose with enhanced gate electric field (Figure 3, right). The degradation in pMOS devices is much less severe since V_{EAp} is still in the range 35...50V after 55Mrad(Si). Very few results are available in the literature concerning the variation with dose of parameters specific to analog designs, and data about g_D are extremely hard to find. In [57], authors mentioned no significant degradation of g_D up to 10Mrad(Si). Two or three dimensional device simulations should be performed to understand the effect of Q_{ox} and D_{it} on V_{EA}.

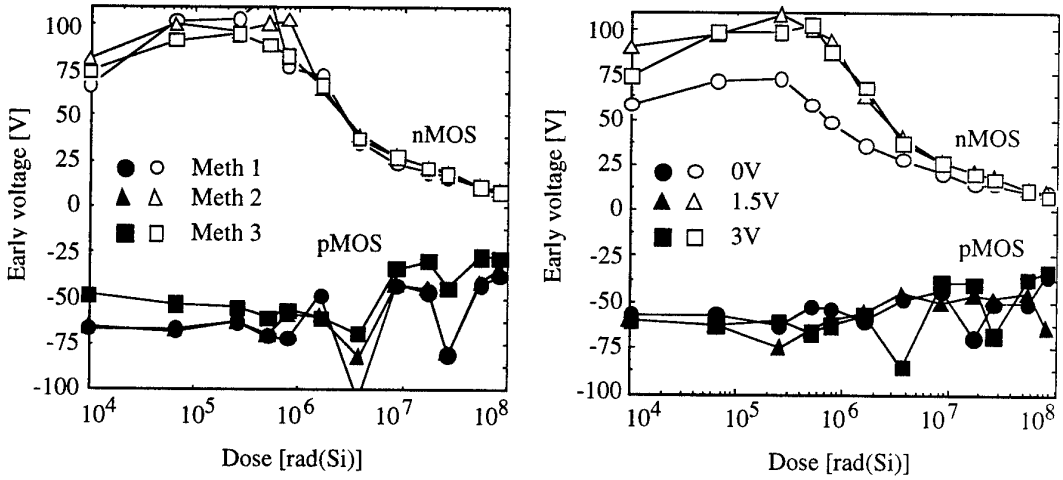

Figure 4: Output conductance as a function of dose in
3μm × 3μm n- and p- channel GAA devices with :
Left: three different extraction methods (presented in Table 5.3) as parameter (V_G = 3V during irradiation);
Right: the gate bias during irradiation as parameter (mean value of the three extraction methods).

Operational amplifiers

Amplifier design

The knowledge of the g_m/I_d and V_{EA} parameters allow one to design an amplifier. An OTA (Operational Transconductance Amplifier) type of architecture was chosen. Figure 5 presents the schematics of such an amplifier.

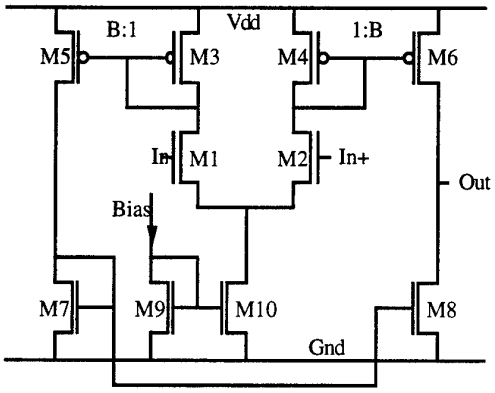

Figure 5: Operational Transconductance Amplifier

Since the g_m/I_d ratio varies much more with the dose when the current flowing through the transistors is low than when the current is larger, we decided to base the design on a relatively large current flowing in the devices (25 and 157 µA for 2 different designs, hereafter referred to as "design A" and "design B"). Table 1 presents the width of the transistors in the amplifier (the length being 3 µm in all cases).

Table 4.1 : Calculated transition frequency, gain, and device width for designs A and B.

	fT (MHz)	Id (µA)	Gain (dB)	M1=M2 (µm)	M4=M6 (µm)	M7=M8 (µm)	M9=M10 (µm)
design A (gm/Id=10)	4	25.1	51.5	56	15	7	10
design B (gm/Id=4)	10	157	43.5	20	40	20	40

The measured fequency response of an amplifier is presented in Figure 6.

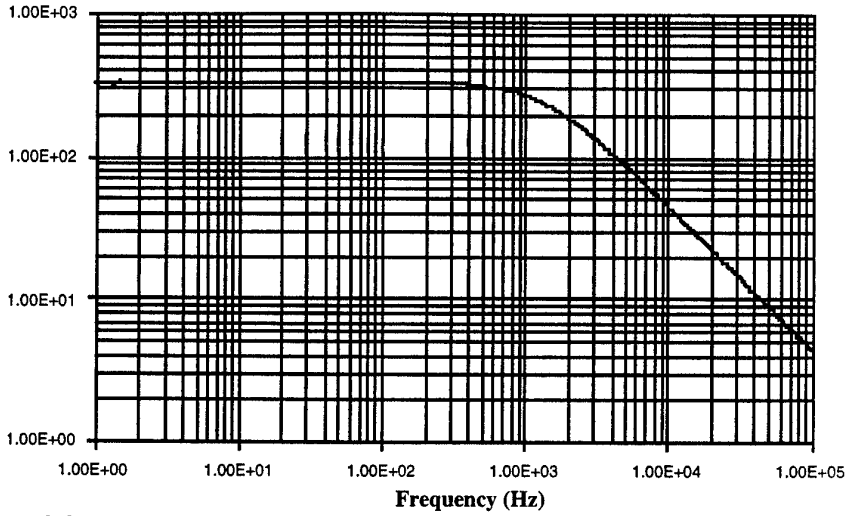

Figure 6: Measured Bode diagram (gain vs. frequency) of an amplifier (design A)

The measured parameters of the amplifiers are compared with the Spice predictions in Table 3.

Table 3: Predicted and measured parameters of the amplifiers.

	Measured		Predicted (Spice)	
	design A	design B	design A	design B
Gain (dB)	50.5	45.3	53.84	42.15
Transition frequency (MHz) (CL=10pF)	2.82	11.88	6.43	10.99
Phase margin (°) (CL=5.25pF)	54.1	64.2	60.39	67.63

Amplifier radiation response

The amplifiers were irradiated using a ^{60}Co source at doses of 41.5 krad(Si), 196 krad(Si), 404.3 krad(Si), 669.3 krad(Si), 1.53 Mrad(Si), 3.36 Mrad(Si), 8.02 Mrad(Si) and 14.37 Mrad(Si). The dose rate was 10krad/h for doses smaller than 1.53Mrad(Si) and 25krad/h for doses higher than 1.53Mrad(Si). The devices were biased during irradiation (bias current = 20 μA). Individual transistors were irradiated as well and measured to assess the effects of dose on their parameters. The variation of the transistor parameters with dose are presented next, for different bias conditions.

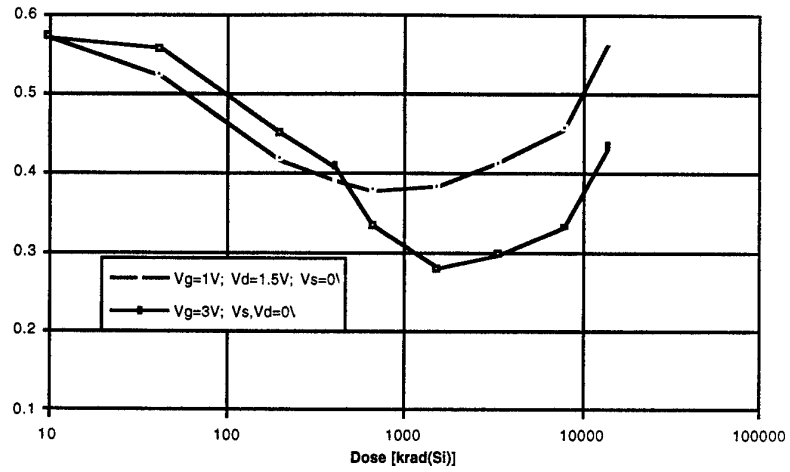

Figure 7: Variation of n-channel device threshold voltage (volts) with dose

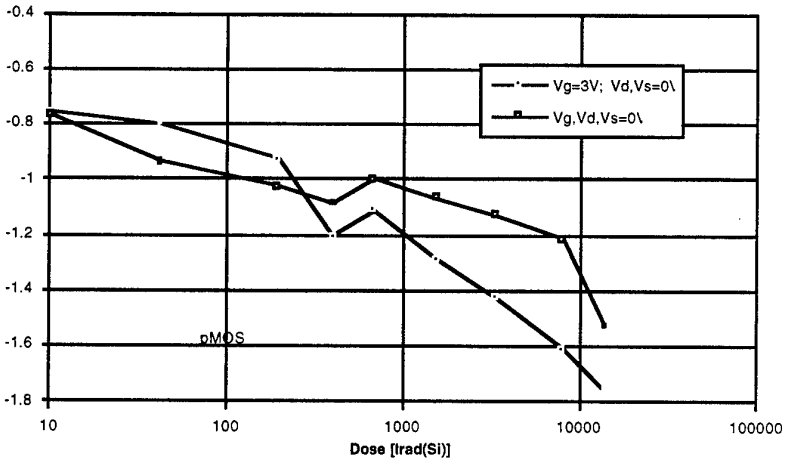

Figure 8: Variation of p-channel device threshold voltage (volts) with dose

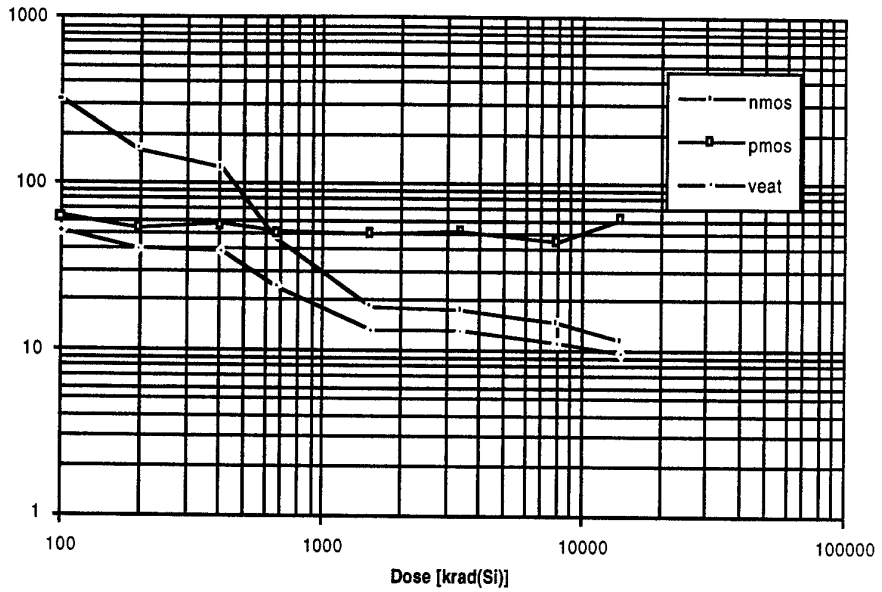

Figure 9: Variation of the early voltage (volts) of n- and p- channel GAA devices with dose, and variation of the equivalent Early voltage of the amplifier based on an output impedance measurement.

The variation of the amplifier parameters with dose are presented next. Four amplifiers were irradiated: two with design A (g_m/I_D = 10 V^{-1}) and two with design A (g_m/I_D = 4 V^{-1}).

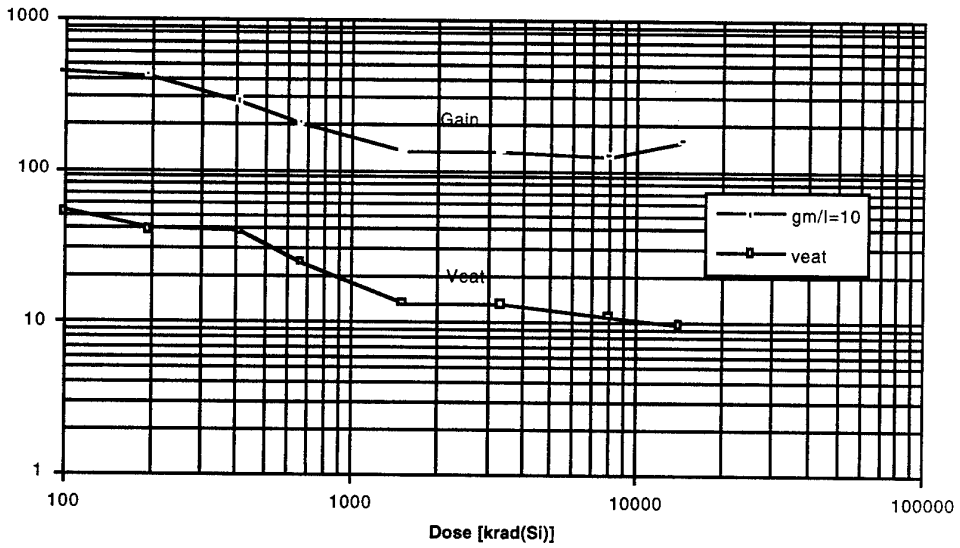

Figure 10: Variation gain of the amplifier (design A) with dose, and variation of the equivalent Early voltage of the amplifier based on an output impedance measurement.

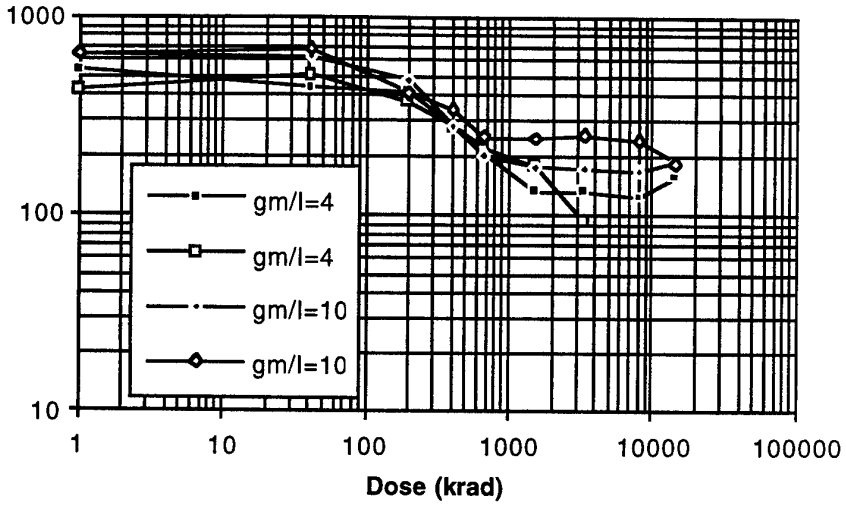

Figure 11: Variation of the gain with dose for the 4 amplifiers

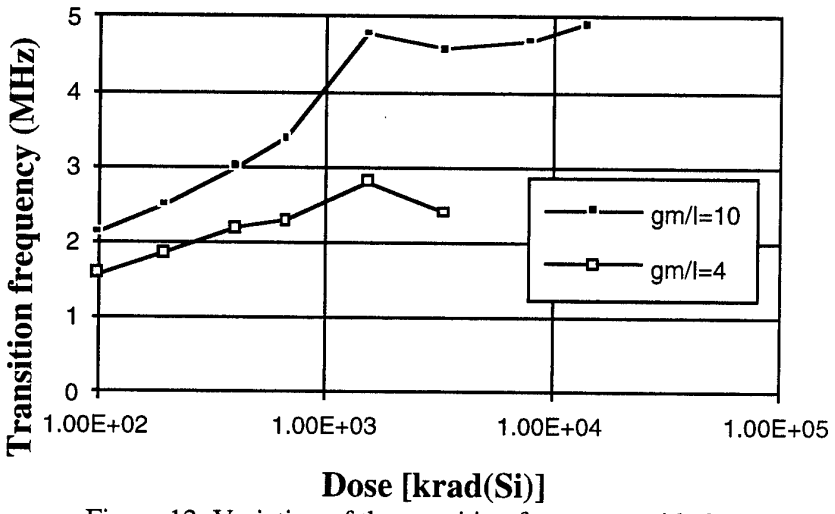

Figure 12: Variation of the transition frequency with dose

Table 4.6: Evolution of the phase margin as function of dose for a A-type amplifier (bias current= 60 μA) and a B-type amplifier (bias current = 340 μA).

Dose	Ibias=60A	Ibias=300A
pre-rad	54.13°	50.9°
44.8krad(Si)	51.29°	50.6°
214krad(Si)	48.5°	50.36°
447.8krad(Si)	48°	50.16°
693.3krad(Si)	47.78°	51.26°
1.57Mrad(Si)	47.8°	52.9°
3.7Mrad(Si)	48.18°	54.36°
5.5Mrad(Si)	48.9°	55.32°

The linearity of the current mirrors of the amplifiers was measured as a function of dose as well. It can be noted that the degradation of the linearity with dose is much smaller in p-channel current mirrors than in n-channel ones. Indeed, a good linearity is maintained down to current levels of 100 pA in p-channel current mirrors, for all doses, while it starts to degrade at currents levels below 1 μA in n-channel current mirrors.

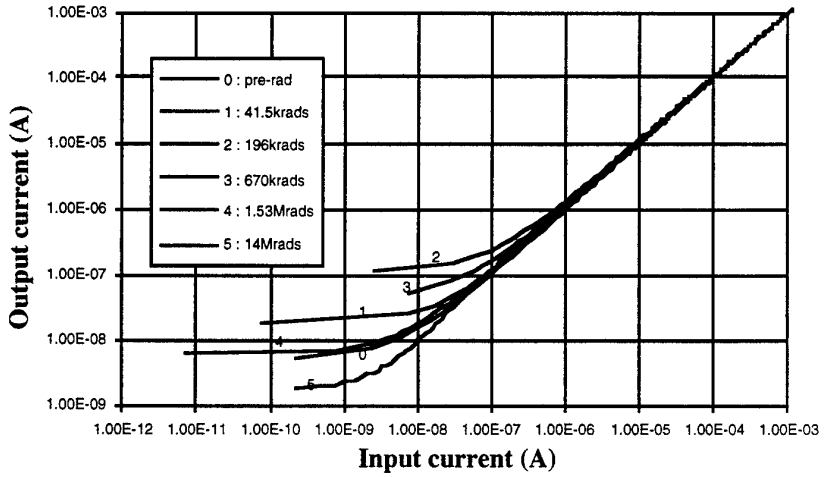

Figure 13: Output vs. input current in an n-channel current mirror

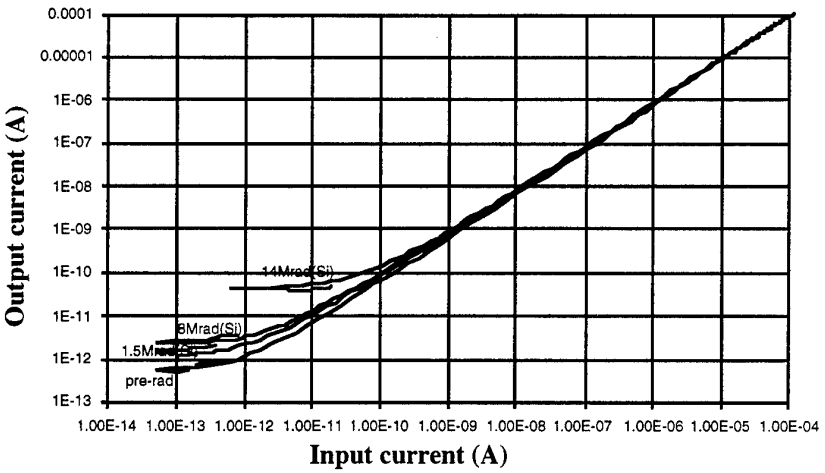

Figure 14: Output vs. input current in a p-channel current mirror

2. Quantum effects in GAA transistors

Two-dimensional electron confinement effects have been modelled and experimentally observed in Silicon-on-Insulator (SOI) Gate-All-Around (GAA) MOSFETs. Solving the Poisson and Schrödinger equations in a self-consistent manner provides the electron wave functions and the energy levels within the device channel. The variation of these energy levels, as well as the electron concentration profile have been computed as a function of gate voltage. Transconductance fluctuations are observed as new energy levels become populated.

INTRODUCTION

The quantum properties of a two-dimensional electron gas (2DEG) have been described for long. Usually, 2D carrier confinement is obtained through the formation of heterojunction structures in III-V compounds or by means of electrostatic confinement. In this Paper, confinement of carriers in silicon is proposed by means of dielectric isolation. Such a confinement is obtained using a Gate-all-Around (GAA) transistor. This device is an SOI MOS transistor where the gate oxide and the gate electrode surround the active channel area.[4] By virtue of the device symmetry, the potential at the top of the silicon film (x=0) is equal to the potential at its bottom ($x=t_{si}$) and the potential minimum is found in the middle of the silicon film, at a depth equal to $t_{si}/2$, where t_{si} is the silicon film thickness.[5] Figure 1 presents the cross section of a GAA transistor.

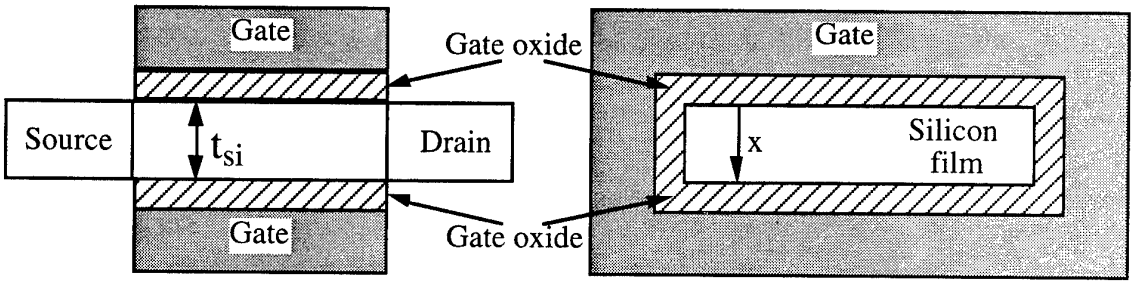

Figure 1: GAA device cross-section: parallel (left) and perpendicular (right) to current flow direction.

In a 2D structure, if the electrons are confined within an infinite square potential well, the permitted energy levels are given by the following relationship: [6]

$$E_\alpha = E_c + \frac{\hbar^2}{2m^*}\left(\frac{\pi\ \alpha}{t_{si}}\right)^2 \qquad (1)$$

4 J.P. Colinge, M.H. Gao, A. Romano, H. Maes, and C. Claeys, "Silicon-on-insulator gate-all-around device", *Technical Digest of IEDM*, P. 595, 1990

5 P. Francis, A. Terao, D. Flandre, and F. Van de Wiele, "Modeling of ultrathin double-gate nMOS/SOI transistors, *IEEE Trans. on Electron Devices*, Vol. 41-5, p. 715, (1994)

6 C.W.J. Beenakker and H. Van Houten, "Quantum transport in semiconductor nanostructures", *in Semiconductor heterostructures and nanostructures, Solid-state physics,* Vol. 44, Ed. by H. Ehrenreich and D. Turnbull, Academic Press, pp. 1-228, 1991

where ħ is the reduced Planck constant, m* is the effective mass of the electron, E_C is the 3D minimum energy of the conduction band, and α is an integer number (α = 1,2,3...). This relation is obtained by the solving of the Schrödinger equation in one dimension in a perfect square potential well:

$$[H_0 + \Phi(x)]\Psi_\alpha = E_\alpha \Psi_\alpha \tag{2}$$

where the Hamiltonian is given by

$$H_0 = -\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2} \tag{3}$$

and where the square well is defined as:

$$\Phi(x) = 0 \text{ for } 0<x<t_{si} \text{ and } \Phi(x) = \infty \text{ for } x<0 \text{ and } x>t_{si} \tag{4}$$

This well-know theoretical problem can be easily solved analytically and yields sine wave functions. Squaring the wave functions provides one with the electron concentration as a function of depth in the silicon film. The total charge distribution, $n_{3D}(x)$, expressed in m^{-3}, can be written as the sum of the electron concentration in each energy subband:

$$n_{3D}(x) = \sum_\alpha n_{2D\alpha}(E_F).\,|\,\Psi_\alpha(x)\,|^2 \tag{5}$$

Where $n_{2D\alpha}(E_F)$ is the 2D electron density corresponding to the permitted energy level E_α for a given Fermi level E_F. The presence of this electron concentration modifies the original potential well, such that the Poisson equation must be used to compute the new potential distribution:

$$\frac{d^2}{dx^2}\Phi(x) = \frac{q\,n_{3D}(x)}{\varepsilon_{si}} \tag{6}$$

This potential must be added to the original square well potential in order to obtain a better estimate of the wave functions.

Such basic formulas are important to understand the 2D conduction phenomena taking place in GAA MOSFETs. In this paper, we would like to start from those theoretical results, extend their scope to a more generalized case and apply them to the particular case of the GAA transistor.

THEORY

The main objective in generalizing the problem is to solve it for any gate potential model, and for a potential well with is no longer perfectly square. This will afterwards allow one to analyze the influence of the doping concentration and study the electron distribution along the x-axis in the inversion layer. However, in order to limit computation time we will take advantage of the device symmetry (Figure 1) and consider that the potential at the top of the silicon film (x=0) is equal to the potential at its bottom ($x=t_{si}$), and that the potetential minimum is found in the middle of the silicon film, at a depth equal to $t_{si}/2$.

At first, the potential configuration in the device has to be computed by means of the Poisson equation applied over the whole GAA structure (the silicon film, and the gate oxide above and below it):

$$\frac{d^2}{dx^2}\Phi(x) = \frac{q}{\varepsilon_{si}}(n(x) + N_a(x)) \tag{7.a}$$

in the silicon, and

$$\frac{d^2}{dx^2}\Phi(x) = \frac{q}{\varepsilon_{ox}}N_{ox}(x) \tag{7.b}$$

in the oxide, and in which n(x) refers to the electron density in the inversion channel and $N_a(x)$ takes into account the depletion charge in the whole structure, if N_a is the acceptor ion doping concentration. N_{ox} is the fixed oxide charge density.

The boundary conditions for the potential are determined at the interface between the silicon dioxide and the gate electrode ($x=-t_{ox}$), where the potential is equal to the gate voltage V_g , and by the symmetry property at the middle of the silicon film ($x=t_{si}/2$):

$$\begin{cases} \Phi(x)=V_g \quad \text{at} \quad x=-t_{ox} \\ \dfrac{d}{dx}\Phi(x)= 0 \ \text{at} \ x=t_{si}/2 \end{cases} \tag{8}$$

The Schrödinger equation to be used is similar to the one previously mentioned when considering the square potential well :

$$\left\{ -\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2} + \Phi(x) \right\} \Psi_\alpha = E_\alpha \Psi_\alpha \tag{9}$$

As previously, the next step to obtain the local electron density is the determination of the density of states for the 2D silicon structure, $\rho(E)$, expressed in $J^{-1}\ m^{-2}$ units: [7]

$$\rho(E) = g_s\, g_v \frac{m^*}{2\pi\hbar^2} = \rho \tag{10}$$

This density depends on the effective mass m* and on the g_s and g_v spin and valley degeneracy factors.

Finally, if we assume operation at the temperature of 0 K, the relation to be calculated in order to get the local electron density (in m^{-2} units) is finally given by equation 11.

$$n_{2D\alpha} = \int_{E_\alpha}^{E_F} \rho(\xi)\, d\xi = (E_\alpha - E_F).\ \rho \tag{11}$$

The actual computation requires the iterative resolution of the Poisson equation, the Schrödinger equation and of the electron density in the inversion layer, in order to obtain a self-consistent resolution method.

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7 T. Ando, A.B. Fowler, and F. Stern, *Review of Modern Physics,* Vol. 54, p. 437, 1982

FORMULATION

The Finite Difference Method is used together with with the mathematical software MATLAB, which is particularly well adapted to matrix calculations.

The total thickness of the GAA device is divided into a 2.*n* mesh elements. Thanks to the symmetry of the device, only *n* points need to be calculated and stored in matrices. This leads to a drastic reduction of the computation time, but calls for a more complex formulation.

The potential in the half device is represented by a vector :

$$\Phi(x)=\left[\Phi_1,\Phi_2,.,.,\Phi_n\right]=\overline{\Phi_i} \quad \text{with } i=1...n \tag{12}$$

which encompasses the potential in the gate oxide, $\overline{\Phi_i}$ for i=*1...(m-1)*, and the potential in half the silicon film, $\overline{\Phi_i}$ with i=*m...n*.

The vector $\overline{\Phi_i}$ extends into the SiO_2 and, hence, the presence of charges in the gate oxide; can be accounted for using an areal potential $\overline{U_{ox}} = \frac{qN_{ox}(x)}{\varepsilon_{ox}}$; for i=*1...m*. In the silicon film the charge is the sum of the depletion charge and the inversion charge gives rise to an areal potential as well:

$\overline{U_{si}} = q\frac{\overline{N_a} + \overline{n}}{\varepsilon_{si}}$; for i=*m-1...n*. $\overline{U} = \overline{U_{ox}} + \overline{U_{si}}$ is the areal potential for the entire structure. On the other hand, the solving of the Schrödinger equation takes place only within the silicon film. Therefore, a reduced vector was used to calculate the wave functions in the silicon region ($\overline{\Psi_i}$, with i=*m...n*).

The Laplace operator, $\overline{\overline{L^S}}$, used in the Poisson equation has to be rewritten in a matrix form as well. This is done by means of the finite difference method, applied to the Laplace operator, with a regular mesh step Δx:

$$\overline{\overline{L^S}} = \frac{d^2}{dx^2} = \frac{1}{(\Delta x)^2}\begin{bmatrix} -2 & 1 & 0 & .. & 0 \\ 1 & -2 & 1 & .. & .. \\ 0 & 1 & .. & 1 & 0 \\ .. & .. & 1 & -2 & 1 \\ 0 & .. & 0 & 2 & -2 \end{bmatrix} \tag{13}$$

For the Schrödinger equation, according to the description of the problem, two different types of matrix operators should be used, the first one provides symmetrical wave functions, while the second one provides anti-symmetrical functions. The matrix of the Laplace operator is therefore either symmetrical:

$$\overline{\overline{L^S}} = \frac{d^2}{dx^2} = \frac{1}{(\Delta x)^2}\begin{bmatrix} -2 & 1 & 0 & .. & 0 \\ 1 & -2 & 1 & .. & .. \\ 0 & 1 & .. & 1 & 0 \\ .. & .. & 1 & -2 & 1 \\ 0 & .. & 0 & 2 & -2 \end{bmatrix} \tag{13}$$

or anti-symmetrical: (equal to Equation (13) where the last row has been modified)

$$\overline{\overline{L^a}} = \frac{d^2}{dx^2} = \frac{1}{(\Delta x)^2}\begin{bmatrix} -2 & 1 & 0 & .. & 0 \\ 1 & -2 & 1 & .. & .. \\ 0 & 1 & .. & 1 & 0 \\ .. & .. & 1 & -2 & 1 \\ 0 & .. & 0 & 1 & -2 \end{bmatrix} \quad (14)$$

In either case, the Poisson equation amounts to :

$$\overline{\overline{L^s}} \;.\; \overline{\Phi} = \overline{U} \quad (15)$$

in which the potential, Φ, is obtained through a simple matrix inversion of relationship (15). Schrödinger's equation is resolved in a similar way. The following eigenvalue and eigenfunction problems have to be solved:

$$\left[-\frac{\hbar^2}{2m^*} \overline{\overline{L^s}} + \overline{\overline{\text{diag}\,\Phi}} \right] . \overline{\Psi_\alpha} = E_\alpha . \overline{\Psi_\alpha} \quad (16)$$

and

$$\left[-\frac{\hbar^2}{2m^*} \overline{\overline{L^a}} + \overline{\overline{\text{diag}\,\Phi}} \right] . \overline{\Psi_\alpha} = E_\alpha . \overline{\Psi_\alpha} \quad (17)$$

where $\overline{\overline{\text{diag}\,\Phi}}$ is a matrix containing the vector $\overline{\Phi}$ on its diagonal and zeros everywhere else. The eigenvalues and eigenvectors are obtained by a single MATLAB command. These eigenvalues correspond to the different energy levels, while their corresponding eigenvectors are the desired wave functions.

The electron density, n, in m^{-3} units, is calculated by means of (5). It amounts to :

$$\overline{n} = \sum_{\alpha} (E_\alpha - E_F) \,.\, \rho \,.\, \overline{\Psi}^{\,2} \quad (18)$$

where α is the number of populated subbands (α=1,2,3,...).

This electron density is re-introduced in Poisson's equation in the areal potential term $\overline{U}$. The iterative search for a new concentration is carried on until the required accuracy is reached. Convergence and stability of those calculations are difficult to be obtained. Therefore, an under-relaxation factor γ is introduced to facilitate convergence: the electron concentration is multiplied by a factor γ before it is re-introduced in the Poisson equation :

$$\overline{n} = \overline{n^{new}}\,(1-\gamma) + \overline{n^{old}}\,\gamma \quad (19)$$

This coefficient γ, which lies between 0 and 1, is computed during each iterative process. It is found experimentally that a small coefficient has to be used to ensure proper convergence (γ=0.05).

Once this convergence is reached, a new set of calculations is restarted for slightly changed V_g boundary conditions.

RESULTS

Simulations were carried out for for a thin (40 nm) and lightly doped (10^{13} boron atoms/cm^3) Gate-All-Around device. The gate oxide is 32 nm thick. The data of actual

GAA transistors measured at low temperature [8] are used for comparison with the simulation.

The device is simulated for various gate voltages. As explained in the introductory part, the density of states in the conduction band of a low-dimensional device is not continuous. Various permitted energy levels appear above the bottom of the conduction band. If a gate voltage is applied, a band curvature and a lowering of the conduction band towards the Fermi energy level are produced. The permitted energy levels, E_α, bend accordingly. When the first permitted level is intercepted by the Fermi it becomes populated by electrons and inversion appears, which corresponds to reaching the threshold voltage, in a classical approach. Figure 2 represents the evolution of the energy levels versus gate voltage. These energy levels are represented with reference to the Fermi level.

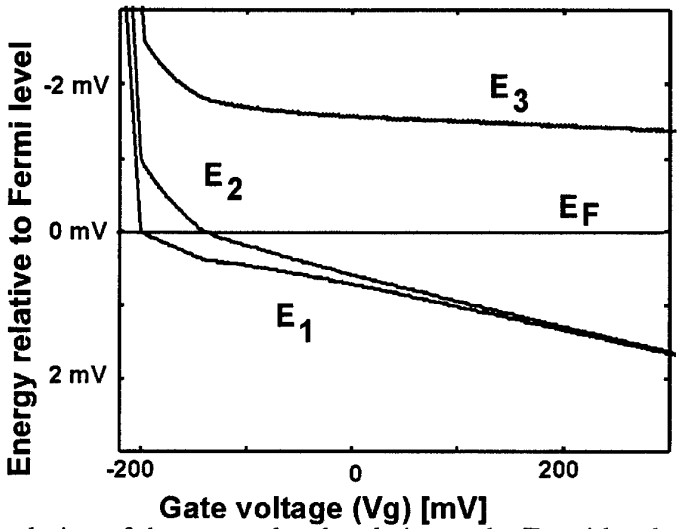

Figure 2 : Evolution of the energy levels relative to the Fermi level as a function of the gate voltage, V_g. For an increasing gate voltage, one can observe the two first energy levels, E_1 and E_2 crossing the Fermi energy level.

The simulation reveals that, before inversion takes place, the various energy levels bend rapidly with the gate voltage, because they closely track the channel potential ($d\Phi(Vg)/Vg \cong 1$). Once the first permitted energy level reaches the Fermi energy, the presence of an inversion channel affects the shape of the potential well and the relative positions of the higher energy levels. Figure 3 shows the modification of several wave functions with gate voltage.

8 J.P. Colinge, X. Baie and V. Bayot, "Evidence of two-dimensional carrier confinement in thin n-channel gate-all-around (GAA) devices", *IEEE Electron Device Letters*, vol. 15, p. 193, 1994

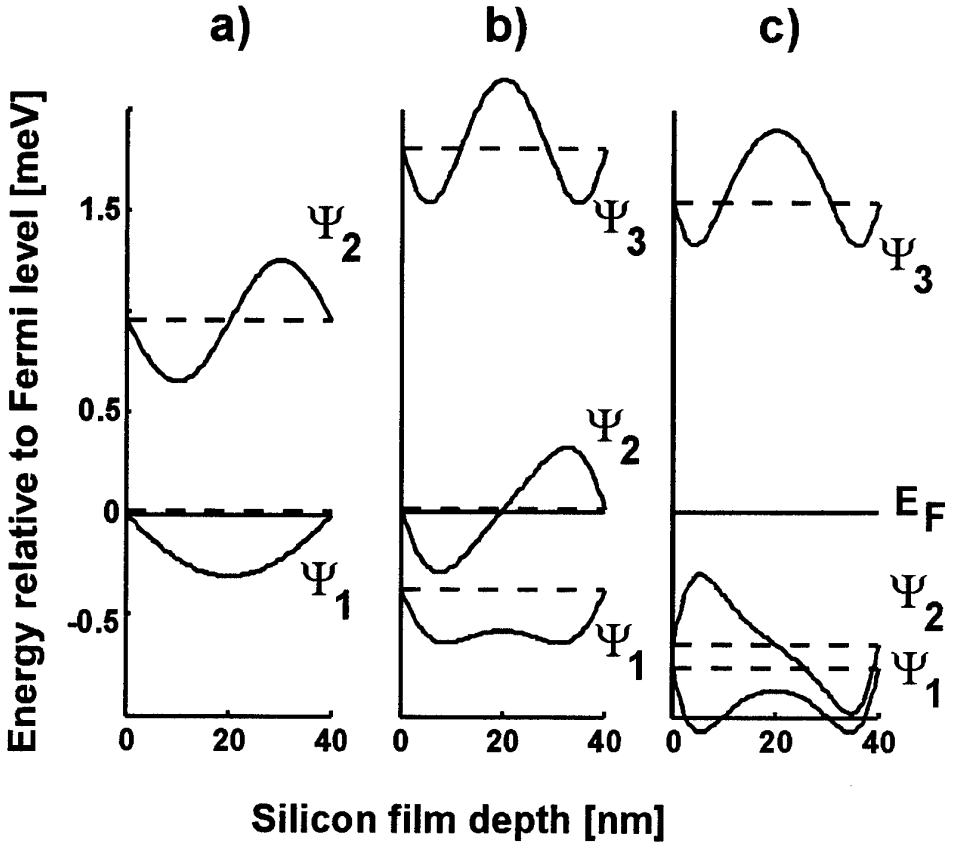

Figure 3 : Evolution of the first wave functions and their respective energy levels as a function of the gate voltage, V_g.

The three graphs of Figure 3 respectively illustrate the situation a) where the gate voltage is lower than the threshold voltage, b) where one permitted energy level is being populated and c) where two energy levels are populated. Figure 3c clearly shows that, when two levels are populated, the two first wave functions have a tendency to pair up, and their energy levels degenerate into a single energy level. One wave function is symmetrical while the other one is antisymmetrical.This effect is due to the curvature of the potential well, which leads to the formation of two inversion channels, close to the Si-SiO_2 interfaces instead of the volume inversion channel which is observed at lower gate voltages.

Figure 4 illustrates the evolution the electron density versus depth in the silicon film for the three different gate voltages. Figure 4a presents the situation where the gate voltage is right above the threshold. Only the first energy level is populated, and most of the free electrons are found in the center of the silicon film. This case illustrates well the concept of volume inversion, first introduced by Balestra *et al.* [9] In Figure 4b the gate voltage is increased in such a way that the second subband is close to become populated. In this case the electrons still all belong to the first subband. One can notice that channels are starting to form at the Si-SiO_2 interfaces. Figure 4c presents the case where the second subband is populated. The formation of two surface channels becomes even more evident, but volume inversion remains present in the center of the silicon film.

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9 F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance", *IEEE Electron Device Letters*, Vol. 8, p. 410, 1987

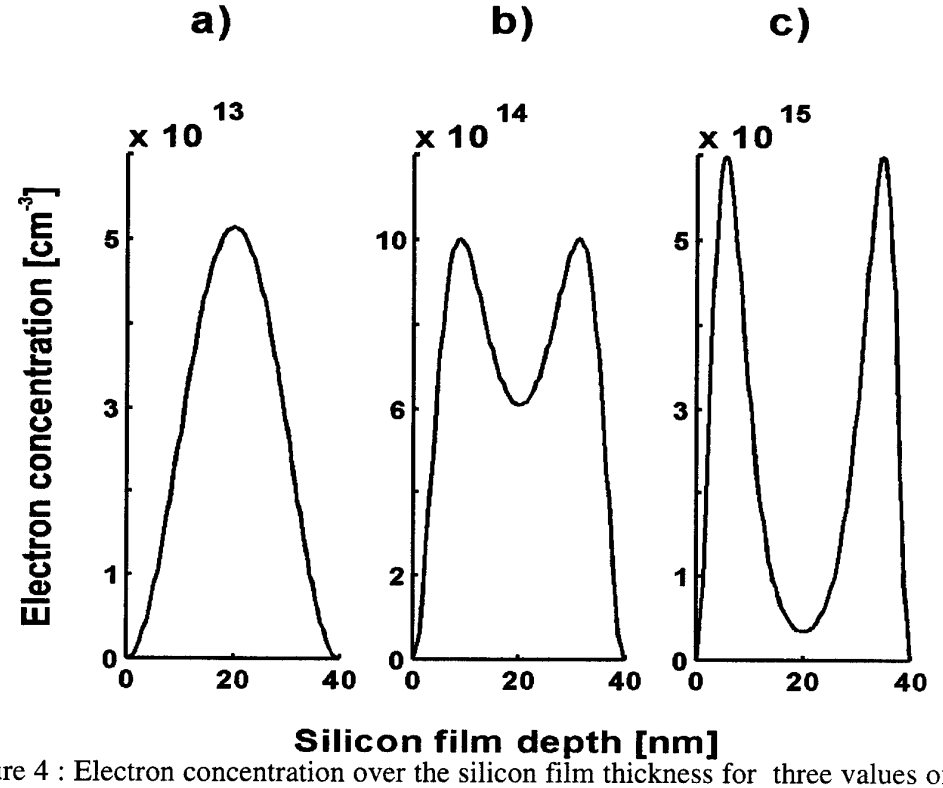

Figure 4 : Electron concentration over the silicon film thickness for three values of the gate voltage: a) right above threshold; b) right before filling of the second subband; c) the second subband is populated.

The local electron density in the film thickness vs. gate voltage is plotted in Figure 5. The mesh points located at the left the darker line correspond to electrons of the first subband only, and, at higher gate voltage it corresponds to electrons populating both the first and the second energy levels. Once again, the volume inversion effect is clearly seen, as well as the formation of two surface channels at higher gate voltages.

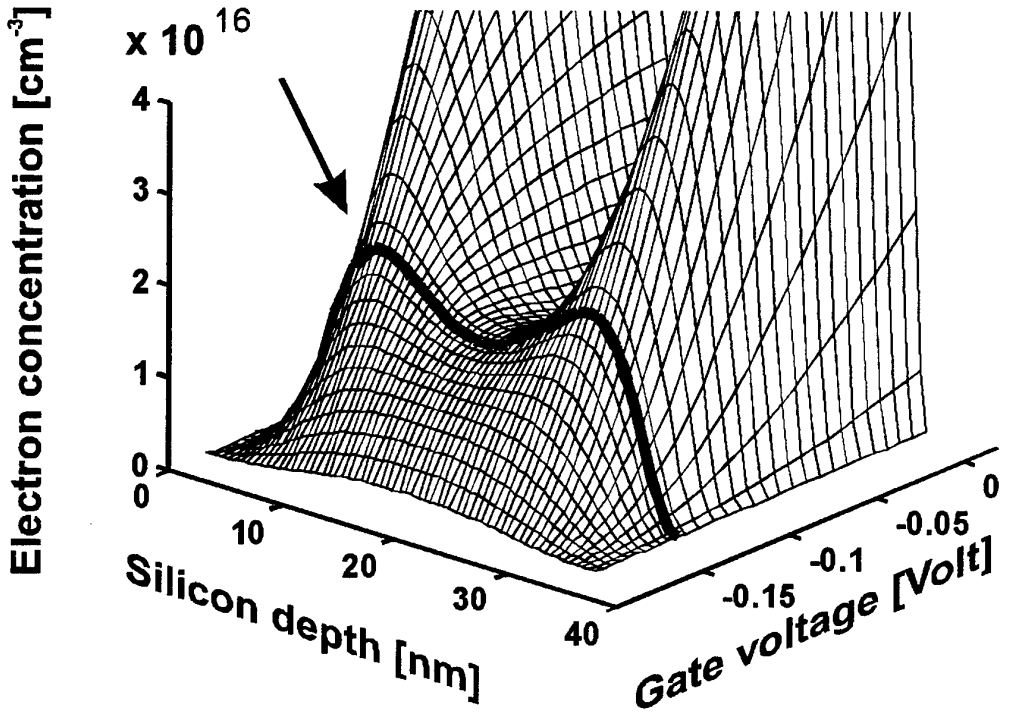

Figure 5 : Electronic concentration in the silicon film versus gate voltage. The arrow is pointing to the increase of conduction when the second energy level becomes populated.

Experimental measurements of the transconductance of a 40 nm-thick transistor were reported in [5], from which Figure 6 is extracted. It can be observed that a peak of transconductance is observed at a gate voltage of V_{th}+100 mV.

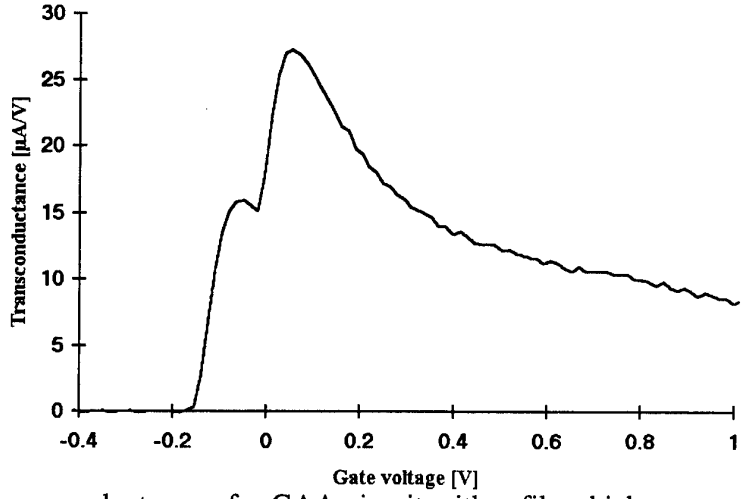

Figure 6 : transconductance of a GAA circuit with a film thickness t_{si} = 40 nm at a temperature of 300 mK and for V_{ds} = 30 mV.

The onset of a drain current at threshold is due to the filling of the first energy subband. At a gate voltage equal to V_{th}+100 mV the second energy level becomes populated. At this moment, inter-subband scattering occurs, which decreases the electron mobility and causes a dip in the transconductance curve. The gate voltage difference between populating the first and the second subbands is 100 mV, which corresponds to the value predicted by the simulation. For larger gate voltage values, no further filling of higher subbands is observed, which is in agreement with the simulation, since the increase of the energy of these levels with gate voltage does not permit them to become populated (Figure 2). Rather, the transconductance curve adopts a classical shape: it reaches a maximum, and then decreases because of scattering of the electron in the channels at the Si-$Si0_2$ interfaces.

The study of the channel doping influence is also fairly interesting. Figure 7 shows the position of the first energy levels versus doping concentration in the channel (N_a varies from 10^{13} to 10^{18} atoms/cm^3) for gate voltages which do not produce an inversion charge charge ($V_g<V_{th}$). The plot represents the modification of the energy levels with reference to the first energy level versus the logarithm of the doping concentration. For low doping concentrations, the doping level has hardly any influence on the position of the energy levels. For higher doping concentrations, the levels E_1 and E_2 tend to come closer to one another, whereas the upper energy levels get away from these two first levels. This phenomenon is due to the curvature of the potential, induced by the depletion charge in the silicon film, which is no longer square-well-shaped at the higher doping concentrations. This simulation therefore emphasizes the need having a low-doped channel to observe subband splitting. Indeed, beside the reduction of impurity scattering defects, the first two levels are more clearly separated and their observation is made easier if the device is lightly doped.

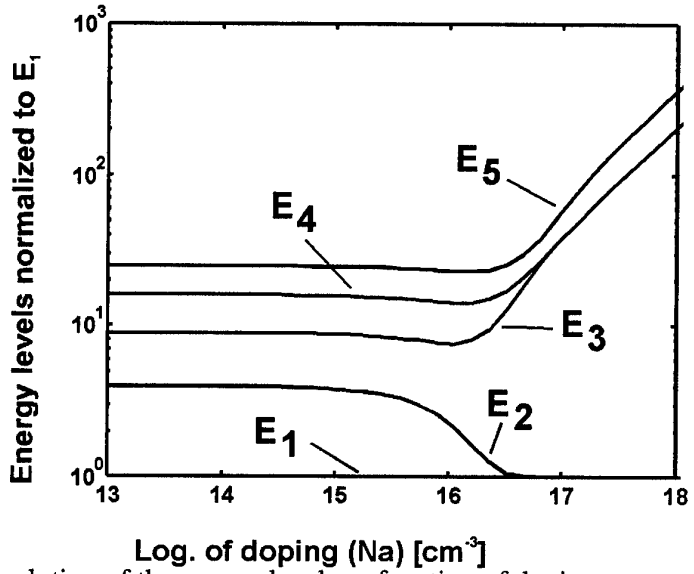

Figure 7 : Evolution of the energy levels as function of doping concentration (relative to the first level E_1).

CONCLUSION

Two-dimensional electron confinement effects have been modelled and experimentally observed in Silicon-on-Insulator (SOI) Gate-All-Around (GAA) MOSFETs. Solving the Poisson and Schrödinger equations in a self-consistent manner provides the electron

wave functions and the energy levels within the device channel. The variation of these energy levels, as well as the electron concentration profile have been computed as a function of gate voltage. Transconductance fluctuations are observed as new energy levels become populated.

3. High-temperature magnetic sensors

This work presents the performances of Silicon-On-Insulator (SOI) CMOS split-drain Hall effect sensors in two implementations operated up to 600K. The first one is the well-known current-voltage converter-like Popovic sensor. The second one is a digital sensor using the analog-to-digital (A/D) double ramp conversion technique. The main advantage of SOI for these applications is the combination of high temperature and low-power, low-voltage features. A particular simulation technique based on MEDICI and DAVINCI is also presented. The simulated electrical field dependence of the relative sensitivity qualitatively reproduces previous analysis.

Introduction

High-temperature magnetic sensors are needed in several applications as position sensor in aeronautics, motor magnetic features and regulation, ... On the contrary to other Hall effect sensors such as bipolar or diode devices. [10,11,12], the Silicon-On-Insulator (SOI) CMOS split-drain sensors combine the advantages of both SOI MOS devices and circuits at high temperature [13,14]. The potential of SOI MOSFETs for high-temperature analog and digital applications has already been demonstrated by many authors. In this study we demonstrate both theoretically and experimentaly the feasibility to implement a split-drain magnetic sensor with current-voltage converter, amplification and offset voltage reduction circuit for application up to 600K. MEDICI and DAVINCI simulations adapted to include magnetic field dependence have been achieved in order to analyze and optimize the sensor sensitivity using a more physical MOS model than previous approaches [15,16].

Devices

We use fully-depleted n- and p-MOSFETs on thin-film SIMOX substrates which are known to have superior device properties for high-temperature operation, i.e. reduced threshold voltage shifts and leakage currents, better output conductance, ... These devices offer additional advantages for designing CMOS circuits. In SOI MOSFETs, the drain leakage current does not flow to the substrate but within the device to the source. Moreover in CMOS opamps or split-drain sensors all devices operate in saturation so that the drain leakage becomes totally negligible. Subsequently, leakage currents can not affect the current biasing, such that power dissipation remains constant with temperature. It also follows that classical circuit architectures need not to be adapted for high-temperature operation and that the low-power designs are not inconsistent with high-temperature requirements.

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10 Popovic, R.S., H.P. Baltes (1983), "A CMOS Magnetic Field Sensor", IEEE JSSC, August, Vol. SC-1, n° 4, p. 426

11 Cristoloveanu, S. (1986), "Integrated Magnetic sensors : An overview", Journal of Electronic Institute of Japan, February, Vol. 13, n°1, p. 87

12 in't Hout, S.R., S. Middelhoek (1993), "High Temperature Silicon Hall Sensor", Sensors and Actuators, Elsevier Sequoia, Vol. 37-38, p. 26

13 Francis, P., A. Terao, B. Gentinne, D. Flandre, J.P. Colinge (1992), "SOI Technology for High-Temperature Applications", Proc. IEDM, p. 353

14 Flandre, D., A. Terao, P. Francis, B. Gentinne, J.P. Colinge (1993), "Demonstration of the Potential of Accumulation Mode MOS Transistors on SOI Substrate for High-Temprature Operation (150-300°C)", IEEE Electron Device Lett., p. 10

15 Popovic, R.S. (1985), "Numerical Analysis of MOS Magnetic Field Sensors", IEEE Solid-State Electronics, Vol. 28, n° 7, p. 711

16 Agrawal, R., P.K. Yadava, R. Dwivedi, S.K. Srivastava (1991), "Analysis of an n-channel MOSFET Magnetic Sensor with Non-Uniform Impurity Profile", Sensors and Actuators, Elsevier Sequoia, Vol. 28, p. 21

The bulk CMOS split-drain sensors are well-known for good performances and CMOS process compatibility. Nevertheless SOI devices offer additional advantages like better impurity profile uniformity and correct operation at high temperature. Moreover SOI allows one to combine low-power, low-voltage and high-temperature sensor operation.

The split-drain MOSFET sensor shown in figure 1a has two drains separated by an isolation region. In the device, a magnetic field perpendicular to the channel causes a Lorentz deflection of the current flow towards one of the two drains. In a first order model, this slight imbalance in the drain current is proportional to the magnetic field. The relative sensitivity defined as

$$S_r = \frac{I_{D1} - I_{D2}}{(I_{D1} + I_{D2})\, B_\perp} \qquad [1/T]$$

is the drain current imbalance to the total device drain current ratio per magnetic field unit where I_{D1} and I_{D2} are the drain currents and $B_\perp$ is the perpendicular component of the magnetic field.

To optimize sensor sensitivity we need a MOSFET simulator including Hall effect magnetic field. Most of the Hall effect simulators only offer an approximated MOS model. On the other hand, 2D MEDICI and 3D DAVINCI simulators allow for the use of good physical device models and fine realistic device meshes but up to now do not include Hall effect. However given a n-type rectangular area diffusion between two electrodes at different potentials, the perpendicular magnetic field produces a lateral deflection of electrons (figure 2a). For a lateral distorsion of the diffusion shape corresponding to the Hall angle θ_H where $\tan(\theta_H) = \mu_H \cdot B_\perp$, with μ_H, the Hall mobility, as shown in figure 2b, the electron current flows in parallel lines [17]. Consequently, in first order, the magnetic field effect on devices as in figure 2a can be emulated by a device lateral torsion without magnetic field as figure 2c. The split-drain MOSFET of figure 1a is used for the initial device mesh generation in MEDICI and DAVINCI simulations. The twisted mesh of figure 1b is then obtained by shifting the node locations in the initial mesh file. A compromise for the choice of torsion angle in the simulation resides between low angles which need very accurate computation and high angles which violate the first-order approximation. The angle value we used is about 0.5° corresponding to about 0.1T.

Figures 3, 4 and 5 present DAVINCI simulations of the relative sensitivity for both SOI and bulk CMOS split-drain devices of 100µm x 100µm (WxL). The simulations are qualitatively valid to the first order. An extensive quantitative study would however be needed to fully qualify this simulation technique. From figures 3 and 4 we can conclude that the relative sensitivity is larger in saturation than in linear region but decreases with mobility reduction with V_G and V_D in agreement with [18]. Moreover split-drain SOI MOSFET relative sensitivity is better than for bulk MOSFETs but is more degraded with electrical field. Obviously the relative sensitivity is more degraded by temperature for the bulk device than for the SOI device due to the substrate leakage current (figure 5).

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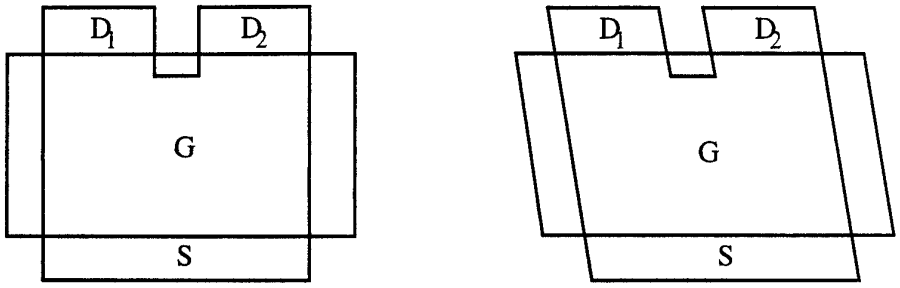
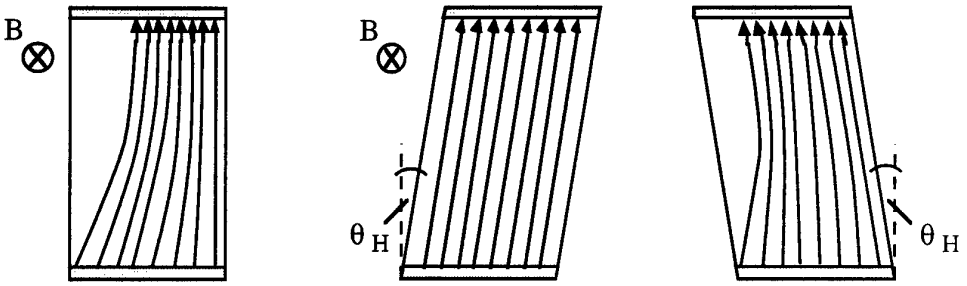
17 Popovic, R.S. (1991), "HALL EFFECT DEVICES : Magnetic Sensors and Characterisation of Semiconductors", Adam Hilger, IOP Publishing Ltd, p. 115

18 Munter, P.J.A., S. Kordic, "The Decrease in the Hall Angle and the Sensitivity of Silicon Magnetic Sensors at High Electric Fields", Sensors and Actuators, Elsevier Sequoia, Vol. 20, p. 225



(a) (b)

Figure 1. Magnetic field split-drain MOSFETs before and after torsion respectively (a) and (b) for MEDICI and DAVINCI simulations.



(a) (b) (c)

Figure 2. Electron flow lines in Hall n-type diffusion plates with magnetic field (a) and (b), without magnetic field (c) and shape torsion (b) and (c).

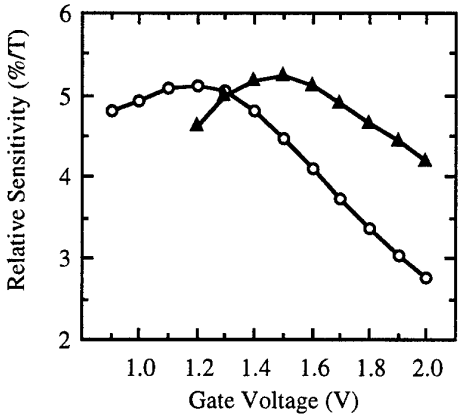


Figure 3. Relative Sensitivity as a function of the Gate Voltage for SOI (O) and bulk (▲) split-drain devices. V_D = 3V, V_{TSOI} =0.85V, V_{TBULK} = 1V.

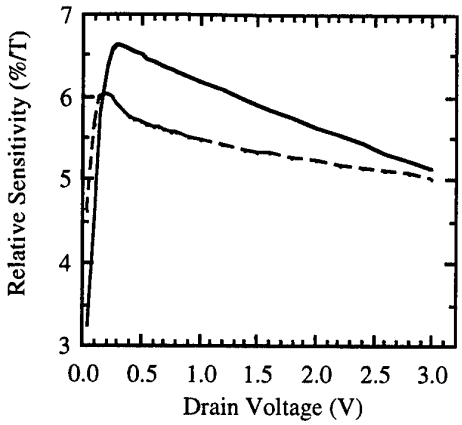


Figure 4. Relative Sensitivity as a function of the Drain Voltage for SOI (–) and bulk (--) split-drain devices. $I_{D1} + I_{D2} = 4nA$.

CMOS sensor circuits

The first sensor implementation is the Popovic sensor (figure 6) where the drain current imbalances of two complementary split-drain n- and p-MOSFETs (MQ_n and MQ_p) in saturation mode are added at the high impedance output node. The absolute sensitivity can be expressed as follows :

$$S = \frac{(I_{Dn1} - I_{Dn2}) + (I_{Dp1} - I_{Dp2})}{(g_{dn} + g_{dp})\, B_\perp} = (S_{rn} + S_{rp})\, V_{ea} \qquad [V/T]$$

where g_{dn}, g_{dp} and V_{ea} are respectively the output conductances of n- and p-MOSFETs split-drain and the equivalent Early voltage corresponding to the parallel combination of both output conductances. The sensitivity was measured to be only about 0.4V/T under a 2V supply voltage and 50μW_e power consumption for our SOI CMOS technology using 15μm x 6μm (WxL) devices. Figure 7 shows the measured influence of the bias current on the sensitivity. The sensitivity improvement with reduction of bias current can be explained by the reduction of both V_G and V_D (figures 3 and 4). The sensitivity per ampere of current consumption unit is 1.6 10^4 V/AT at room temperature and is larger than bulk performance with 10V supply voltage. The measured sensitivity is only 4 times lower at 600K than at room temperature (figure 8) due to the mobility reduction with temperature and the slightly temperature dependence of the MOSFETs output conductances.

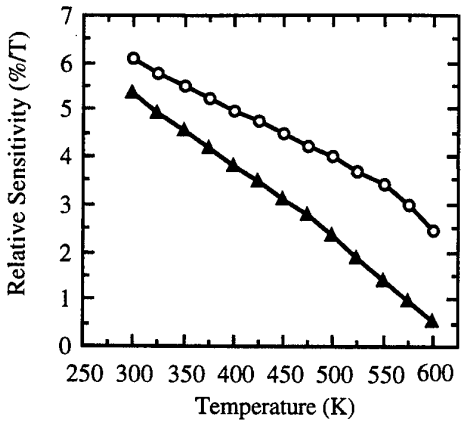


Figure 5. Relative Sensitivity as a function of Temperature for SOI (O) and bulk (▲) split-drain devices. $I_{D1}+I_{D2}$ (300K) = 4nA, V_D = 1.5V.

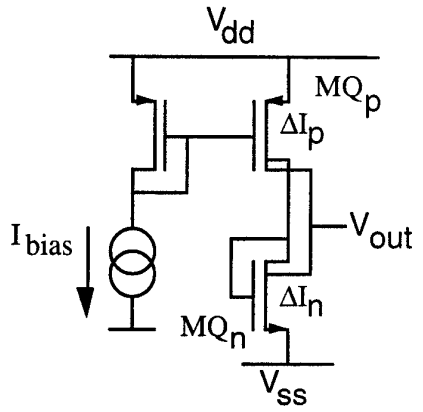


Figure 6. Popovic CMOS magnetic field sensor.

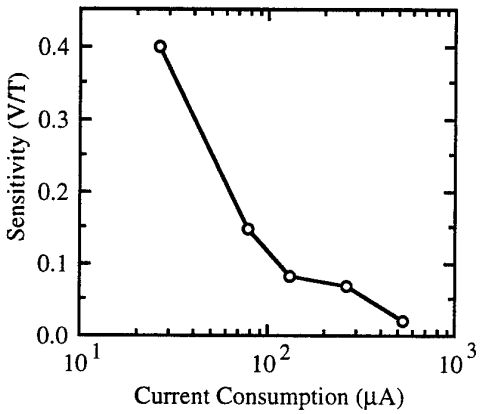


Figure 7. Measured Sensor Sensitivity as a function of Current Consumption at room temperature.

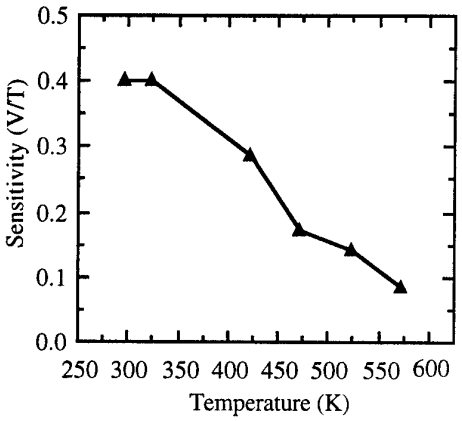
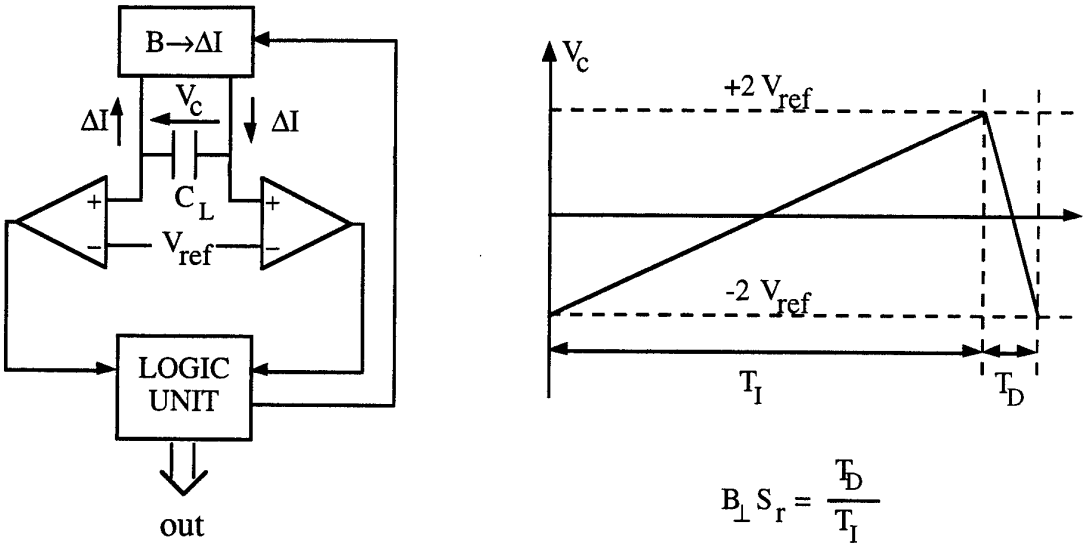


Figure 8. Measured Sensor Sensitivity as a function of Temperature.

A second SOI CMOS split-drain sensor implementation is a high temperature digital sensor based on the analog-to-digital (A/D) double ramp conversion technique. In the first step the split-drain sensor drain current imbalance is integrated on the capacitor C_L up to a reference voltage detected by a comparator (figure 9). In the second step a reference current equal to the total sensor current discharges the capacitor. Consequently the discharge time to integration time ratio corresponds to the magnetic field - relative sensitivity product. The split-drain can be considered as a CMOS differential input pair in a fully-differential folded-cascode CMOS transconductance amplifier (figure 10). The integration capacitance is connected to the differential output nodes. The common mode feedback (CMFB) is realized by the transistors M1 and M2. In the integration step, the switches S_1, S_2 and S_3 are on and differential current issue from the split-drain MOSFET is integrated on the capacitance C_L. In the second step, the sensor is switched off by S_1 and the capacitance is discharged by a differential reference current created by switching off either S_2 or S_3 under the logical unit control.

The one-chip implementation includes the split-drain sensor, additional offset canceling circuit using two opposed split-drain sensors, integration capacitance and two comparators. The logic part with the counter is external. The digital sensor is designed for 600K temperature operation under 2V power supply voltage. The expected performances are summarized in table I.



(a) (b)

Figure 9. Schematic diagram of the digital magnetic field sensor (a) and capacitance voltage drop as a function of the time in two conversion steps .

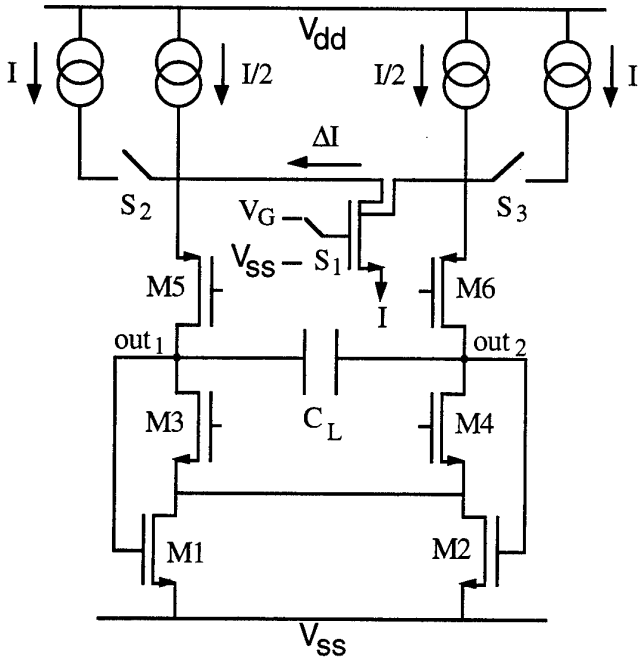


Figure 10. Main circuit diagram of the digital magnetic field sensor.

Supply Voltage:	2V
Power consumption :	60μWe (main circuit)
	30μWe (comparator)
Conv. time (B=0.1T) :	300μs (T=300K)
	900μs (T=600K)
Accuracy :	8 bits

Table I. Digital magnetic field sensor performance summary.

Conclusion

SOI CMOS split-drain sensor MEDICI and DAVINCI performance simulations using a physical MOS model and a special mesh to emulate the magnetic field were presented up to 600K. Split-drain SOI MOSFETs are more sensitive at room and high temperature that bulk MOSFETs but are more dependent of electrial field. Two low-power sensor circuit implementations have been realized and discussed. A reduction of sensor sensitivity by a factor 4 is observed between 300K and 600K corresponding to the temperature dependence on the mobility.

4. Tungsten metallization on $TiN/TiSi_2$

Self-Aligned TiN barrier layer formed by RTN (Rapid Thermal Nitridation) of $TiSi_2$ in ammonia has been studied and applied on thin-film SOI (Silicon-On-Insulator) devices with tungsten metallization system for high-temperature applications. The optimized RTN temperature for such kind of application was found at about 920°C. The leakage current with $W/TiN/TiSi_2/Si$ structure was almost the same as that of Al/Si structure at both room temperature and high temperature (320°C). Even after a 920°C-10sec annealing, the thin-film SOI MOSFETs with the new metallization system still worked correctly. No excessive leakage was observed after thermally stressing the sample wafer at 420°C in forming gas for 2 hours.

Introduction

Thin-film SOI (Silicon-On-Insulator) MOSFETs are considered to be good candidates for both analog and digital applications at elevated temperatures (>250°C) owing to their superior high temperature properties, such as low leakage current, low threshold voltage shift, etc. [19] But at high temperatures, aluminum is no longer a reliable metallization system because of its significant electromigration. Tungsten was proposed to be a replacement of aluminum for high density and long life requirement at high temperature.[20] In a previous work, we have demonstrated a tungsten metallization system on thin film SOI devices for high temperature applications.[21] But even with a contact layer of $TiSi_2$, which is used in thin film SOI technology to reduce the S/D series resistance, tungsten still can react with silicon to form WSi_2 during RTA (Rapid Thermal Annealing) process at temperatures higher than 800°C. In the worst case, the very thin silicon layer in thin-film SOI structures will be totally consumed by tungsten to form silicide which destroys the thin-film SOI devices.

TiN layers formed by rapid thermal nitridation of $TiSi_2$ in ammonia have been proved to be an effective barrier layer between aluminum and silicon [22,23,24]. In this work, the nitridation reaction on a thin $TiSi_2$ layer will be studied, and a self-aligned $TiN/TiSi_2$ contact structure will be applied on thin-film SOI devices as a barrier layer for tungsten metallization system. No significant reaction between tungsten and silicon was observed after high-temperature annealing.

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19 Auberton-Hervé, A.J., J.-P.Colinge and D. Flandre, "High-Temperature Applications of SIMOX Technology", Japanese Solid-State Technology, Dec. 1993, pp.12-17

20 Brusius, P., B.Gingerich, M.Liu, B.Ohme, and G.Swenson, "Reliable High-Temperature SOI Process", Transaction of Second International High-Temperature Electronics Conference, Charlotte, NC, USA, June 1994, ppII 15-19

21 Chen, J. and J.-P.Colinge, "Tungsten Metallization Technology for High-Temperature Silicon-On-Insulator Devices", Materials Science and Engineering, B29 (1995) pp18-20

22 Ku, Y.H., E.Louis, D.K.Shih, S.K.Lee, D.L.Kwong and N.S.Alvi, "Stable, Self-Aligned $TiN_xO_y/TiSi_2$ Contact Formation for Submicron Device Applications", Appl. Phys. Lett., 50 (22), 1 June 1987, pp1598-1600

23 Kamgar, A., F.A.Baiocchi, A.B. Emerson, T.T.Sheng, M.J.Vasile and R.W.Haynes, "Self-Aligned TiN barrier Formation by Rapid Thermal Nitridation of $TiSi_2$ in Ammonia", J.Appl.Phys. 66(6), 15 September, 1989, pp2359-2401

24 Shinriki, H., T.Komiya, N.Takeyasu and T.Ohta, "Selective CVD-Al Contact Plug on Rapid Thermal Processed $TiSi_2$ in NH_3 for High Speed CMOS Using Salicide Process", Extended Abstract of SSDM'94, Yokohama, Japan, 1994, pp946-948

RTN experiment

The nitridation was carried out with an ADDAX XM4 RTA (Rapid Thermal Annealing) system. A 30nm-thick titanium layer was deposited on p-type silicon substrates. The first RTA was carried out in a nitrogen ambient, at 675°C for 60sec, to form a high-resistivity C49 phase $TiSi_2$ layer. The TiN layer and unreacted titanium were then removed by chemical etching using a $H_2SO_4+H_2O_2$ mixture. The second RTA was carried out in an ammonia ambient, from 900°C to 1000°C for 20sec to 60sec, to form a self-aligned TiN layer and to transform the $TiSi_2$ layer to its low-resistivity C54 phase, simultaneously.

The formation of a TiN layer can be confirmed by sheet resistance measurement after immersing the sample wafers in dilute HF solution, because the etch rate of TiN in a dilute HF solution is much lower than that of $TiSi_2$. The sheet resistance measurement results of the sample wafers with different nitridation conditions are shown in figure 1 and figure 2. In figure 1, it is clear that there is almost no TiN formed at 900°C for 60sec in nitrogen. All the $TiSi_2$ layer is etched away in 20 sec. The sample wafers annealed in ammonia gas are stable in 2% HF solution for at least 30sec. That confirm the formation of a thin TiN layer on the top of $TiSi_2$ layer. And the thickness of TiN is proportional to the nitridation time. (Figure 2)

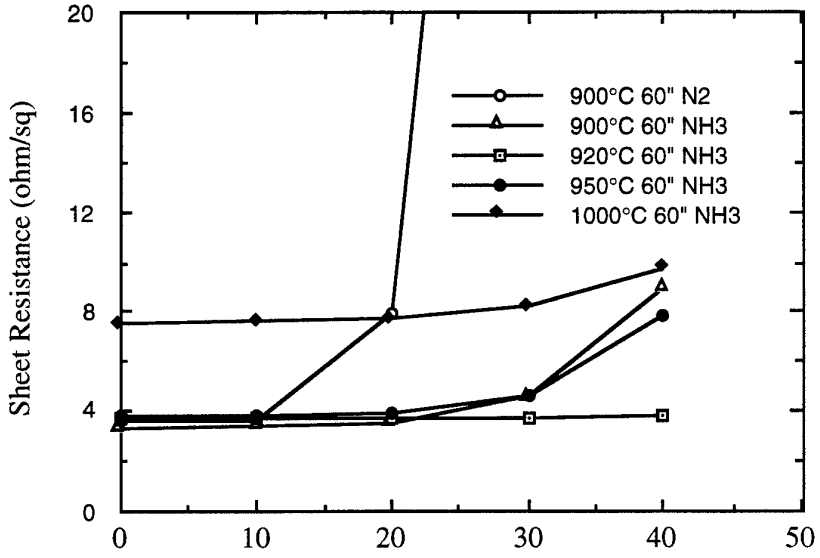

Figure 1: Sheet resistance vs. etching time in 2% HF solution with different nitridation conditions.

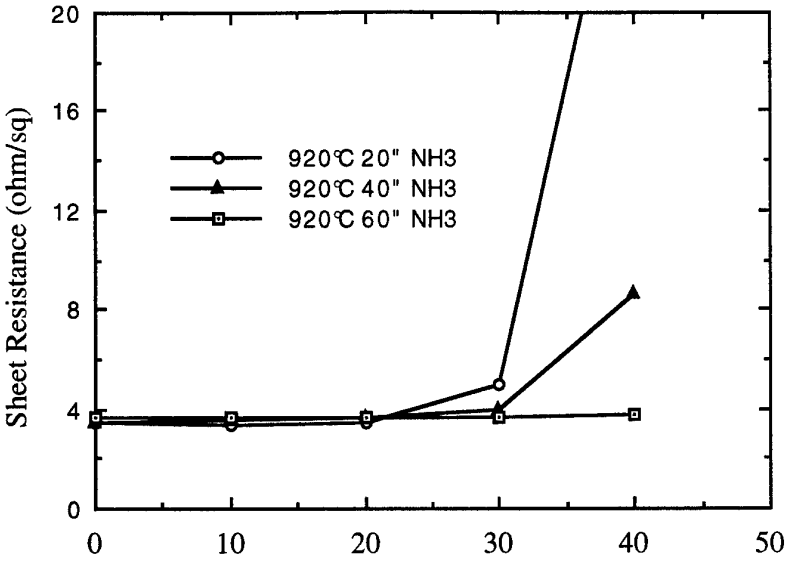

Figure 2: Sheet resistance vs. etching time in 2% HF solution with different nitridation time.

It was reported that (Kamgar, 1989) a 95nm-thick $TiSi_2$ layer could completely be converted into TiN at 1000°C for 60sec in ammonia gas. In our experiments, a significant increase of sheet resistance (the resistivities of TiN and C54 phase $TiSi_2$ layer are about 50--100μΩ.cm and 15--20μΩ.cm, respectively) is also observed after a 1000°C-60sec annealing. But the color of the sample wafer is very faint gold (the color of a pure TiN layer is gold), and its stability in dilute HF solution is similar to that of other wafers annealed at lower temperatures. It is believed that the sheet resistance increase is owing to the agglomeration of the thin $TiSi_2$ layer [25] instead of the total conversion from $TiSi_2$ to TiN. This kind of degradation should be avoided by using lower annealing temperature. Actually, the optimized nitridation condition is found to be at 920°C for 60 sec. in our experiments.

Device fabrication process

Thin-film SOI MOSFETs are fabricated with a CMOS-compatible process on SIMOX wafers. The initial 200nm silicon film is reduced to about 100nm by oxidation and oxide strip. After a LOCOS isolation is used, a 30nm gate oxide is grown. 340nm-thick polysilicon is deposited (LPCVD), doped (implantation, As, 100keV, $1x10^{16}cm^{-2}$) and patterned. Arsenic and boron are implanted to form the sources and drains. Then, a 150nm-thick SiO_2 layer is deposited and etched by RIE to form spacers. After a short-time 2% HF dip, a 30nm-thick titanium layer is deposited on the wafer. The first rapid thermal annealing is carried out at 675°C for 60sec in N_2. TiN layer and unreacted titanium are removed by chemical etching using a $H_2SO_4+H_2O_2$ mixture. The rapid thermal nitridation is carried out at 950°C for 20sec with NH_3. A nitride/oxide layer is then deposited and contact holes are opened to access the devices. 600 nm of tungsten is deposited using an e-gun system with an acceptable step coverage (Figure 3). Tungsten then is patterned with SF_6 plasma etching, (Chen, 1995) and 500nm of SiO_2 is deposited as a passivation layer. A 400nm-thick aluminum layer could be deposited on the contact

25 Lasky, J.B., J.S.Nakos, O.J.Cain, and P.J.Geiss, "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of $TiSi_2$ and $CoSi_2$", ED-38, No. 2, February, 1991. pp262-269

pad to improve the contact property with probes or bonding wires. The final active silicon thickness is around 80nm.

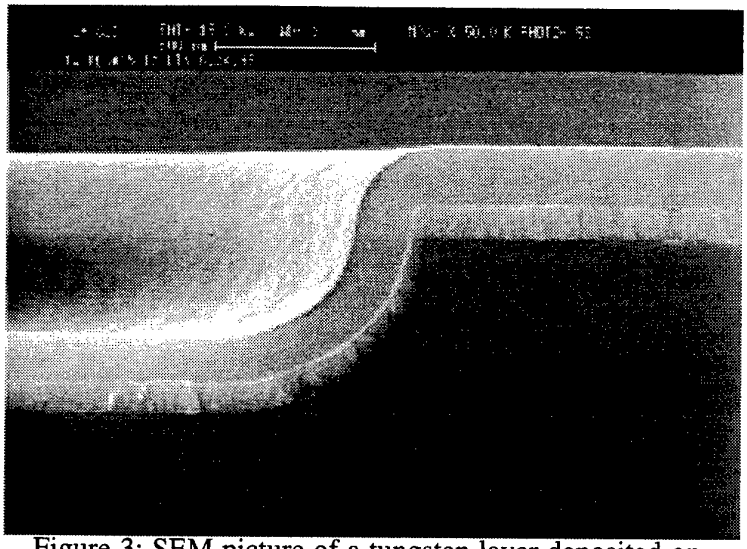

Figure 3: SEM picture of a tungsten layer deposited on the steps by e-gun coating system. (with an SiO2 capping layer)

Transistor characterization

The thin-film SOI MOSFETs are characterized by probe measurement. It is found all the transistors without a TiN barrier layer fail to work after a high-temperature (>800°C) annealing, because the thin silicon layer is totally consumed by tungsten in this case, which destroys the devices. On the contrary, the SOI MOSFETs with TiN/$TiSi_2$ contact structure work correctly even after a 920°C-10sec annealing. The leakage currents are almost the same as that with aluminum metallization system at both room temperature and high temperature (Figure5a, b). No excessive leakage is observed after thermally stressing the sample wafer at 420°C with forming gas for 2 hours. It confirms that the rapid thermal nitridation formed TiN/$TiSi_2$ layer is an effective barrier for tungsten metallization system in thin-film SOI MOSFETs.

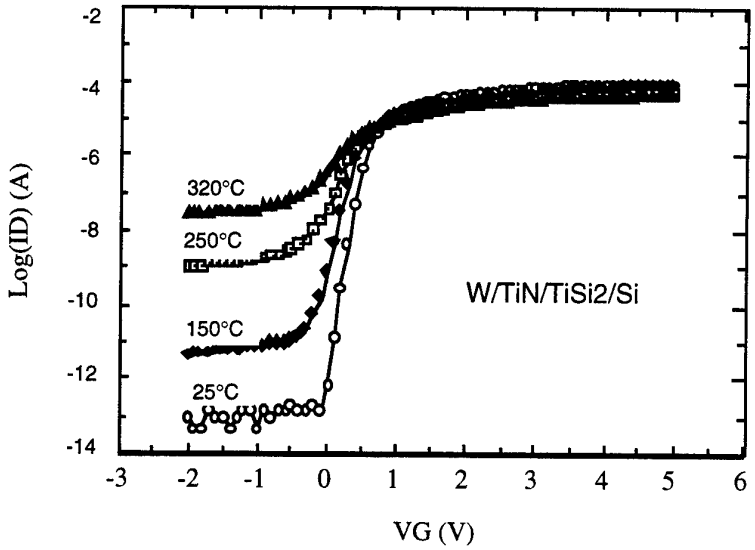

Figure 5a

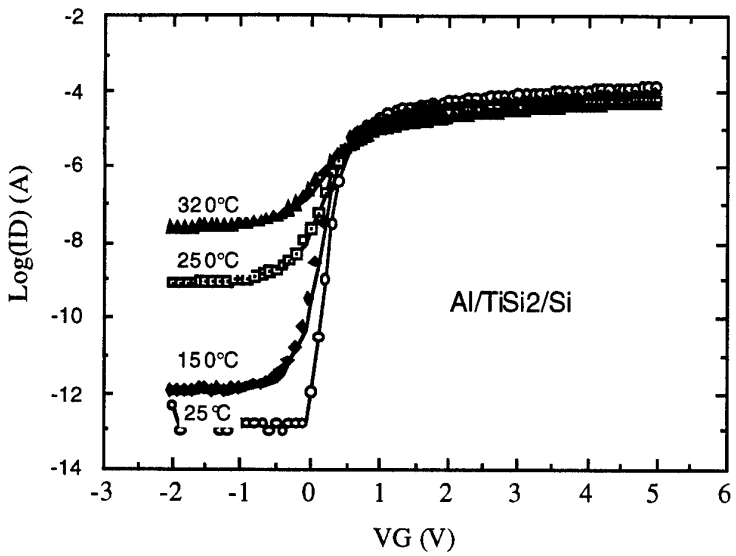

Figure 5b

Figure 5: ID-VG curve of thin-film SOI nMOSFETs with tungsten (a) and aluminum (b) metallization system at different temperatures. The drain voltage V_D is equal to 0.1V. The width and length of the transistors are 20μm and 3μm respectively.

Conclusion

TiN layer formed by rapid thermal nitridation of thin $TiSi_2$ in ammonia gas has been studied and applied on thin-film SOI MOSFETs as a barrier layer for tungsten metallization system. The optimized nitridation temperature in this application is found to be around 920°C. The thin-film SOI MOSFETs using tungsten metallization system with a TiN/$TiSi_2$ contact structure have the similar leakage current as those with aluminum metallization system. Even after a 920°C-10sec annealing, the transistors still work correctly. No excessive leakage is observed after a 400°C-2hour thermal stressing in forming gas.

5. SOI quantum wires

Thin silicon films insulated from bulk silicon by a buried SiO_2 layer are a good starting material for quantum device fabrication. A quantum wire array has been realized and measured at low temperature. The quantum-wire MOSFETs have been realized using e-beam lithography. As expected the current increases with the gate voltage in a stairway-like manner which is characteristic of a 1DEG structure. A finite element method simulator has been used to solve self-consistently the Poisson and Schrödinger equations and obtain the electron concentration in the cross section of the wires. For different gate voltages wave functions as well as energy levels, electron concentration and potential distribution can be evaluated. This shows, for low gate voltage values, a degeneracy of the first wave functions and the variation of the energy levels. Computed energy levels and band filling agree well with low-temperature measurements made on the wires.

Introduction

Electrons confined in a one-dimensional electron gas (1DEG) or a two-dimensional electron gas (2DEG) can be observed in the channel of a MOSFET. For these structures the conduction band splits into several subbands at different energies. In these cases, the permitted energy levels for electrons take the values E_a [26][27]:

$$E_\alpha = E_c + \frac{\hbar^2}{2m^*}\left(\frac{\pi\ \alpha}{t_x}\right)^2$$

for a two dimensional electron gas confined in the x direction, in a thickness t_x.
And values $E_{a,b}$:

$$E_{\alpha;\beta} = E_c + \frac{\hbar^2}{2m^*}\left(\left(\frac{\pi\ \alpha}{t}\right)^2 + \left(\frac{\pi\ \beta}{w}\right)^2\right)$$

for devices were the channel between source and drain looks like a Quantum Wire (1DEG) and where t and w are the confined thickness and width. (m* is the effective electron mass; $\hbar$ is the reduced Plank constant; E_c is the bottom of the conduction band and α,β take integer values:1,2,3,...).

When the gate voltage is increased the Fermi potential can cross these energy levels and subbands become populated. When a new subband becomes populated, a new current channel appears.

Measurements

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26 C.W.J. Beenakker and H. Van Houten, "Quantum transport in semiconductor nanostructures", *in Semiconductor heterostructures and nanostructures, Solid-state physics,* Vol. 44, Ed. by H. Ehrenreich and D. Turnbull, Academic Press, pp. 1-228, 1991

27 T. Ando, A.B. Fowler, and F. Stern, *Review of Modern Physics,* Vol. 54, p. 437, 1982

In order to observe quantum effects in our relatively large devices, electrical measurements must be carried out at low temperature. Indeed, the energy spreading at the Fermi level due to higher temperature would mask the onset of a new subband channel in the measured data.

In a Quantum Wire, 1DEG confinement can be easily observed. Subband fill filling is observed directly in the drain current vs. gate voltage curves. Figure 1 shows this curve for different temperatures.

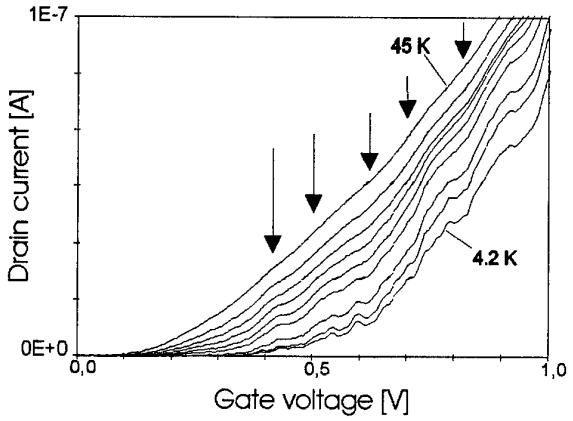


Figure 1: Drain current vs. gate voltage in a Quantum Wire (section = 80 by 100nm) at different temperatures.

The measured device is 80nm thick and 100nm wide. One can see that the gate voltage difference between the onset of first and second subband filling is approximately equal to 100mV.

Simulation

One approach in the interpretation of these measurements is to compare the observed current channel onset with calculation. This comparison can be done based on the evolution of the subbands with gate voltage. The values of the energy of the subbands must be calculated like the energy of an electron confined in a potential well. But the filling of the first band induces a charge increase and an perturbation of the potential. This variation of the shape of the potential induces an energy shift of the subband levels. This shift induces a variation in the filling of the band and electrons concentration. A self-consistent calculation method must, therefore, be used.

Equations to be solved

The 1DEG device must be studied by a resolution in two-dimensional space. To be able to solve any wire cross-section geometry, a finite element method is chosen.
The equations which must be taken into account are the Poisson equation and the Schrödinger equation. The total electron concentration due to band filling must be taken into account in the expression of th Poisson equation.

The Poisson equation is discretized over the geometry of the device. Static charge and doping (depletion) charge are represented by the N(r) charge concentration while n(r) represents the charge of free electrons.

$$\nabla^2 \Phi(r) = \frac{q}{\varepsilon(r)} (n(r) + N(r))$$

The gate voltage is taken into account as boundary condition at the edges of the mesh. The potential, $\Phi(r)$, can be extracted for each node in the structure, and $\varepsilon(r)$ is the permittivity at position r).

The Schrödinger equation may be computed only in the silicon. This reduces both the mesh size and the computing time.

$$[H_0 + \Phi(r)] \cdot \Psi_\alpha(r) = E_\alpha \cdot \Psi_\alpha(r)$$

For each potential shape, the permitted energy levels, E_α, and their corresponding wave functions, $\Psi_\alpha(r)$, are calculated. The total free electron concentration is the sum of the electron concentrations in all subbands.

$$n(r) = \sum_\alpha \left[|\Psi_\alpha(r)|^2 \int_{E_\alpha}^{\infty} \boldsymbol{dos}(\varepsilon)\, \boldsymbol{fd}(\varepsilon;T°)\, d\varepsilon \right]$$

In each subband, the electron distribution is obtained from the squared wave function, $|\Psi_\alpha(r)|^2$, and the electron concentration is obtained, taking into account the degree of filling of the subband. The latter fluctuates with the energy level value, E_α , the density of state in this subband, $\boldsymbol{dos}(\varepsilon)$, and Fermi-Dirac distribution, $\boldsymbol{fd}(\varepsilon,T°)$, at the Fermi level.

Simulation results

Similar results can be obtained in a 1DEG simulation. Figure 2 shows that, for an increase of gate voltage, energy levels cross the Fermi level and subband become populated. Only the ten first levels are plotted.

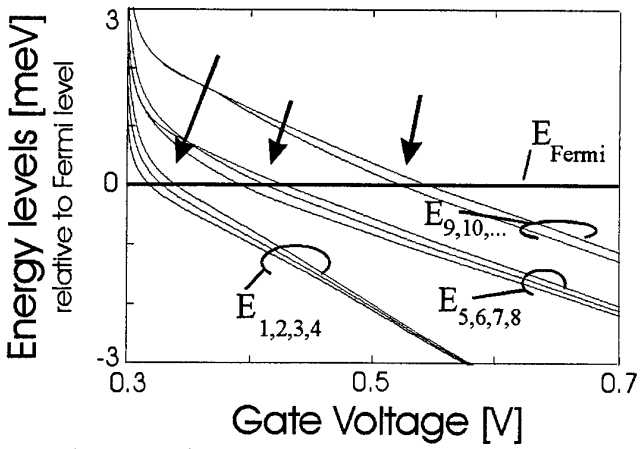


Figure 2: Energy levels shift relative to Fermi level for 1DEG. Temperature: 4K. Square cross section of the wire (100nm by 100nm). Computed by finite elements method.

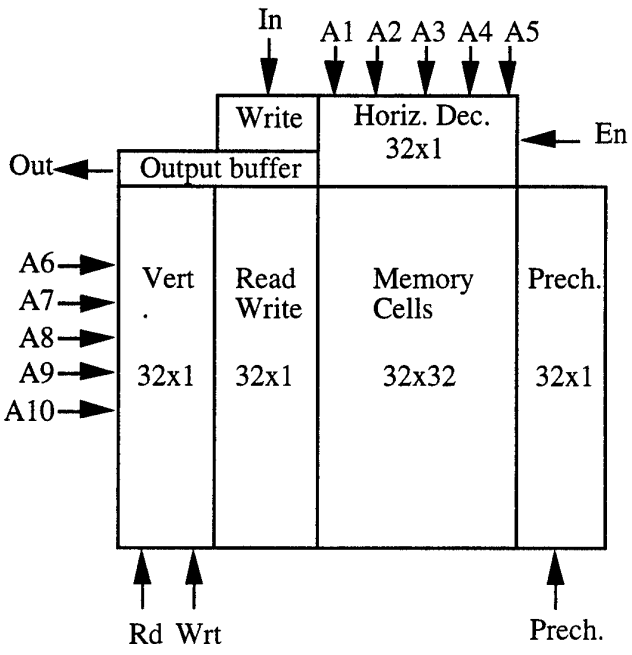
The regularly spaced energy before the first threshold, degenerates quickly for higher gate voltages. The figure shows three groups of degenerated energies. The arrow point out the crossing of the energy levels and Fermi level for each group. These thresholds are 100mV spaced. This value can be related to the 100mV measured in the experiment (figure 2). Other simulations for other cross-section geometry of the wire show strong variations in the position of the onset of the subband filling.

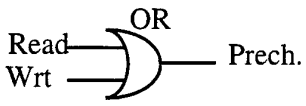
6. Packaged devices

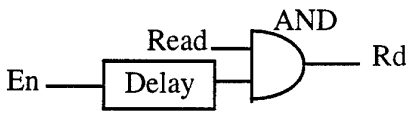
Some packaged devices are provided with this report: GAA 1k SRAMs, GAA operational amplifiers, GAA analog-to-digital converters, and SOI transistors with tungsten metallization. The data sheets for the different devices are presented in the following pages.

1k GAA SRAM Data Sheet

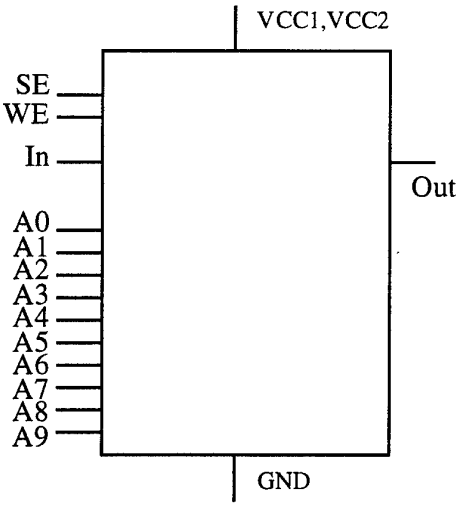
Design:



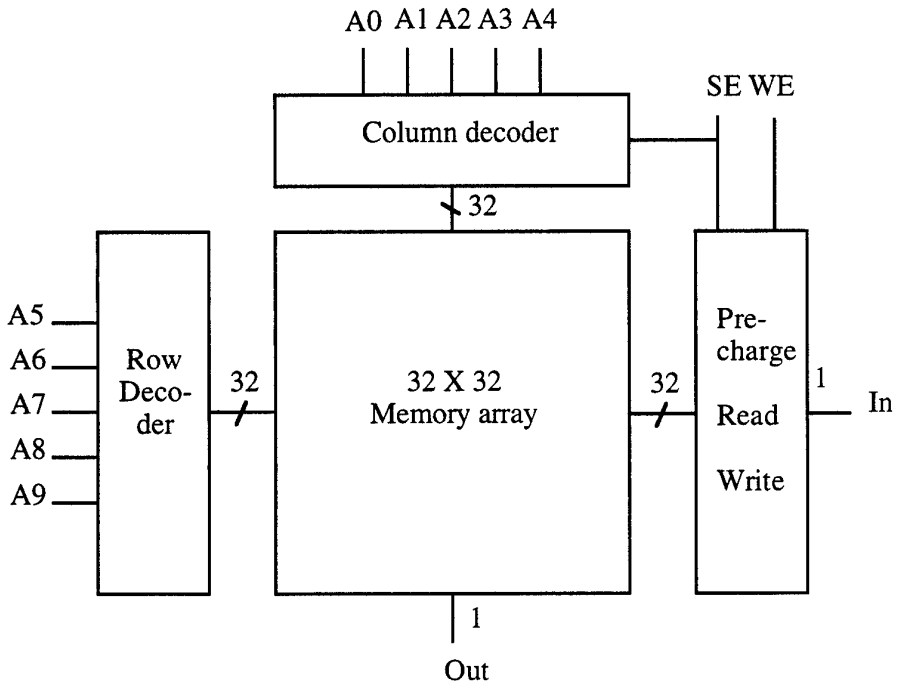




Logic symbol:

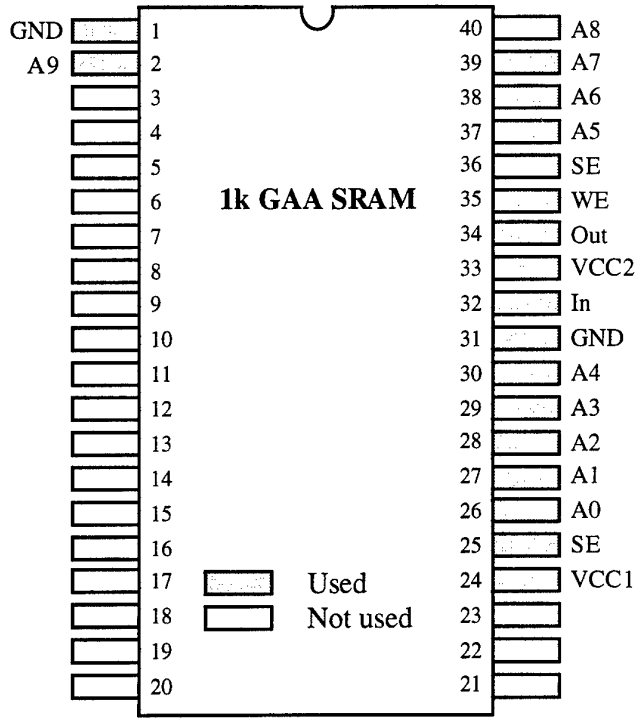


Block diagram:



Package:

Pinout DIL 40 pins (top view)



Pin names:

A0-A9	: Address inputs
In	: Input
Out	: Output
VCC1	: Power (for all except output buffer)
VCC2	: Power of output buffer
GND	: Ground
SE	: Select Enable
WE	: Write Enable

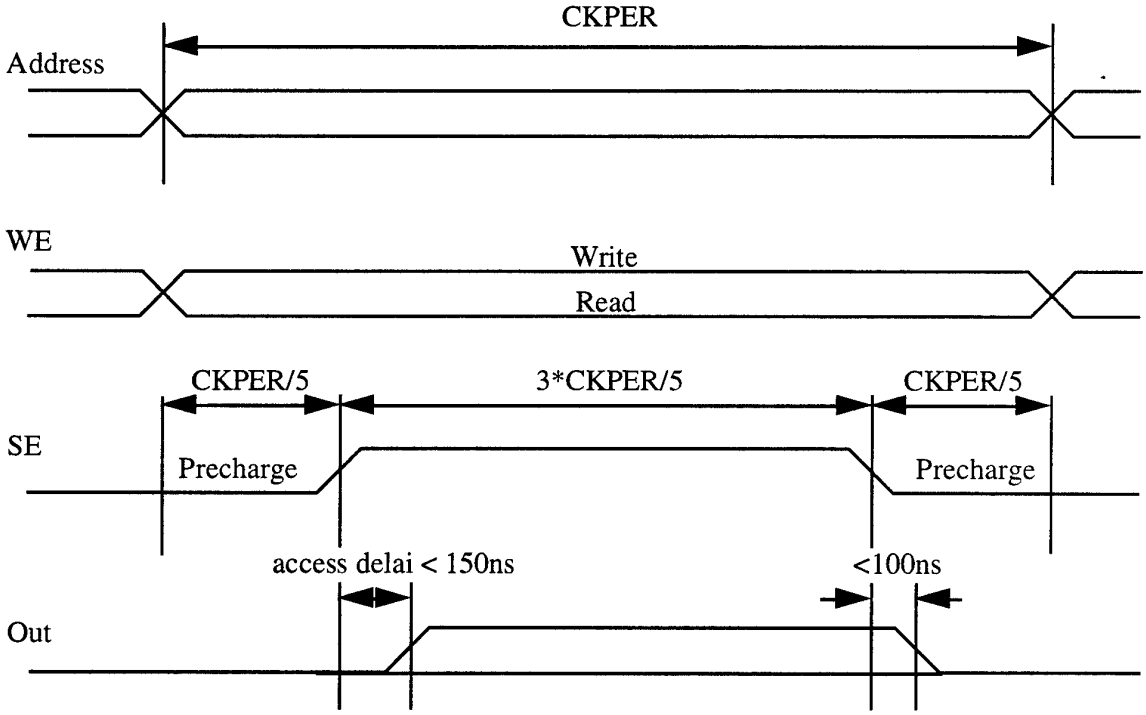
Truth table:

SE	WE	In	Out	MODE
L	L	x	L	Precharge
H	L	x	Data out	Read
H	H	Data in	Data out	Write

L: low
H: high
x: L or H

Timing:

Here is the timing diagram we used. It is preferable to work with the clock period **CKPER > 1µs** with an output capacitance of 8pF and Vdd=3V.



Electrical characteristics:

The supply voltage must be **1.6V < VCC < 3V**, in order to avoid avalanche phenomenon (upper bound) or misfunctionment due to glitches in the supply voltage (lower bound).

Comments:

The output pin is never in high impedance state, the output logic state is low in the precharge mode (Out=L when SE=L).

Pins are not protected against electrostatic discharge.

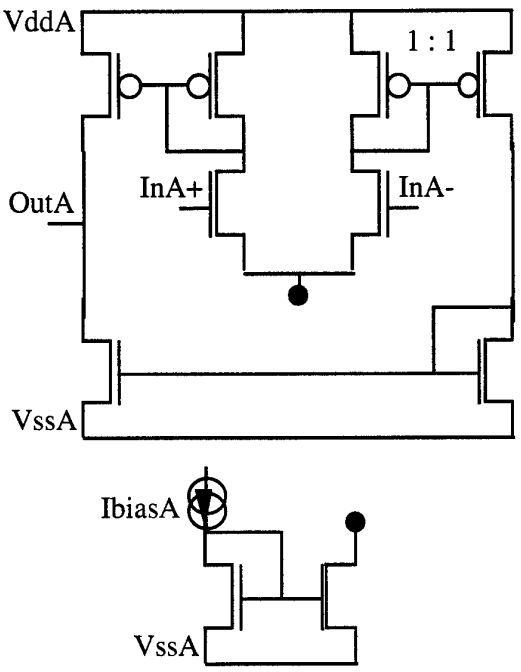
Devices supplied:

One 1k GAA SRAM chip is in the DIL package labeled G23/4

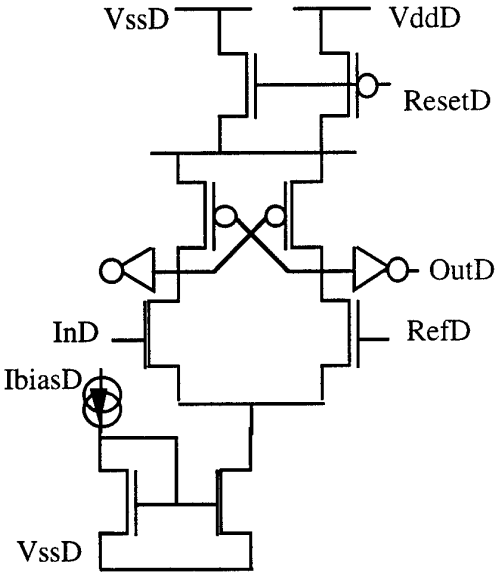
Sigma-delta A/D converter and op-amp

Design:

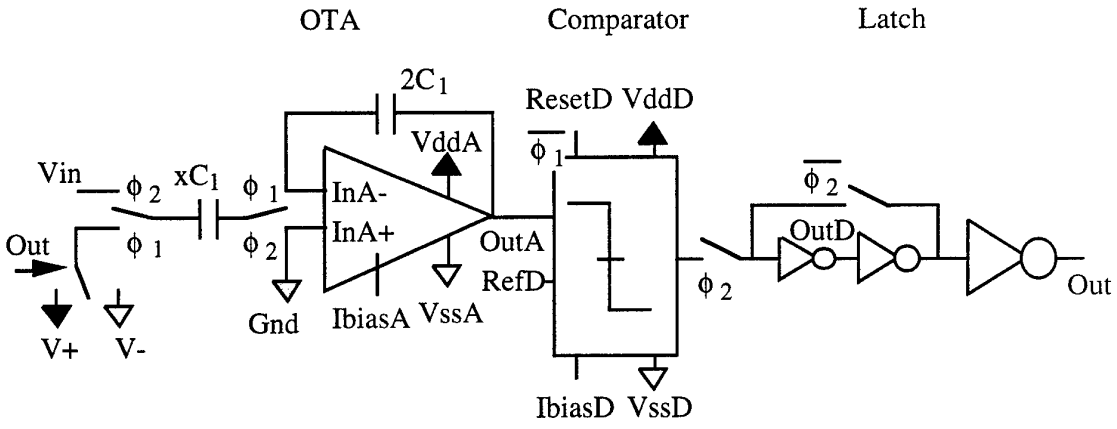
One-stage operational amplifier



Comparator

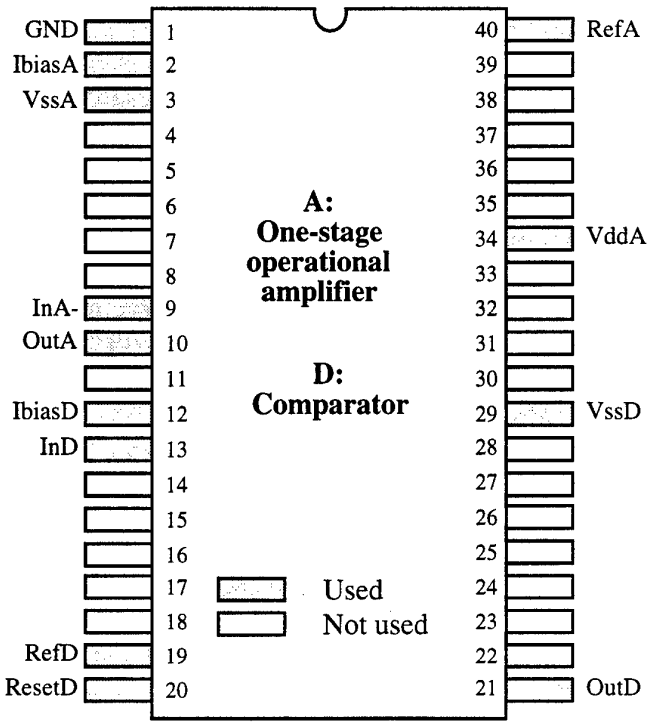


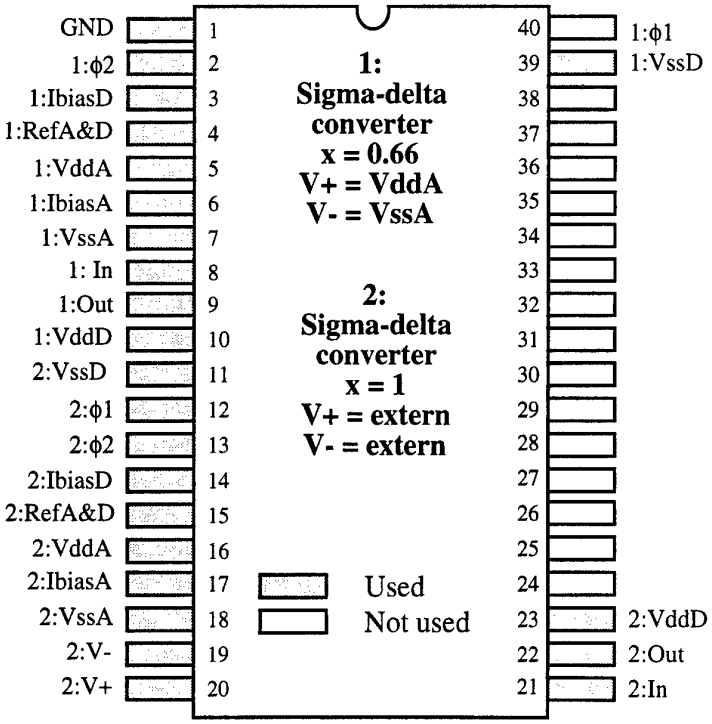
Sigma-Delta converter



Packages:

Pinout DIL 40 pins (top view)





Pin names:

GND	: Ground	: 0V
RefA&D	: Mid-range voltage	: 0V
VddA&D	: Positive supply voltage	: +1.5V
VssA&D	: Negative supply voltage	: -1.5V
IbiasA	: OTA supply current : 10µA	
IbiasD	: Comparator supply current : 10µA	
In	: Input voltage of the A/D converter	
InA-	: Input voltage of the OTA	
InD	: Input voltage of the comparator	
Out	: Output voltage of the A/D converter	
OutA	: Ouput voltage of the OTA	
OutD	: Output voltage of the comparator	
ResetD	: Reset clock of the comparator	
$\phi 1$, $\phi 2$	: Non-overlapping clock of the A/D converter	

Predicted performances:

Simulations performed with hspice predict the following characterisitcs:

OTA: Since C1 = 1pF, the amplifier is optimized with C_{load} = 4pF.

Supply voltage: -1.5V / +1.5V
D.C gain: ~300
Transition frequency: ~4MHz
Phase margin: 74°
Optimum Ibias: ~10µA

Sigma-delta converter:

Supply voltage: -1.5V / +1.5V
$F_{sampling}$: 100 -> 500kHz

Devices supplied:

3 chips containing one GAA op-amp+ and 1 GAA comparator: packages G91/2, G91/2 and G92/2
3 chips containing two GAA sigma-delta converters: packages G91/1, G92/1 and G92/1

Devices with tungsten metallization

Devices supplied:

4 chips containing 4 SOI n-channel MOSFETs with different gate lengths (in µm in the table below), 4 SOI p-channel MOSFETs with different gate lengths (in µm in the table below), one polysilicon-tungsten contact chain, one p-diffusion-tungsten contact chain, and one n-diffusion-tungsten contact chain. The chips are labeled: A, B, C and D. They are identical.

Pin layout:

The packages are 24-pin DIL ceramic packages. The lids are attached using scotch tape, so, please remove them before high-temperature testing!

Type	W/L	Gate	Source	Drain
nMOSFET	20/3	(2)	(1)	(3)
nMOSFET	20/5	(2)	(1)	(24)
nMOSFET	20/10	(2)	(1)	(23)
nMOSFET	20/20	(2)	(1)	(22)
pMOSFET	20/3	(11)	(12)	(13)
pMOSFET	20/5	(11)	(12)	(14)
pMOSFET	20/10	(11)	(12)	(15)
pMOSFET	20/20	(11)	(12)	(16)

Poly contact chain	(4)------(9)
p-dif contact chain	(5)------(8)
n-dif contact chain	(6)------(7)